High-Voltage GaN-Based Half-Bridge Converter Design

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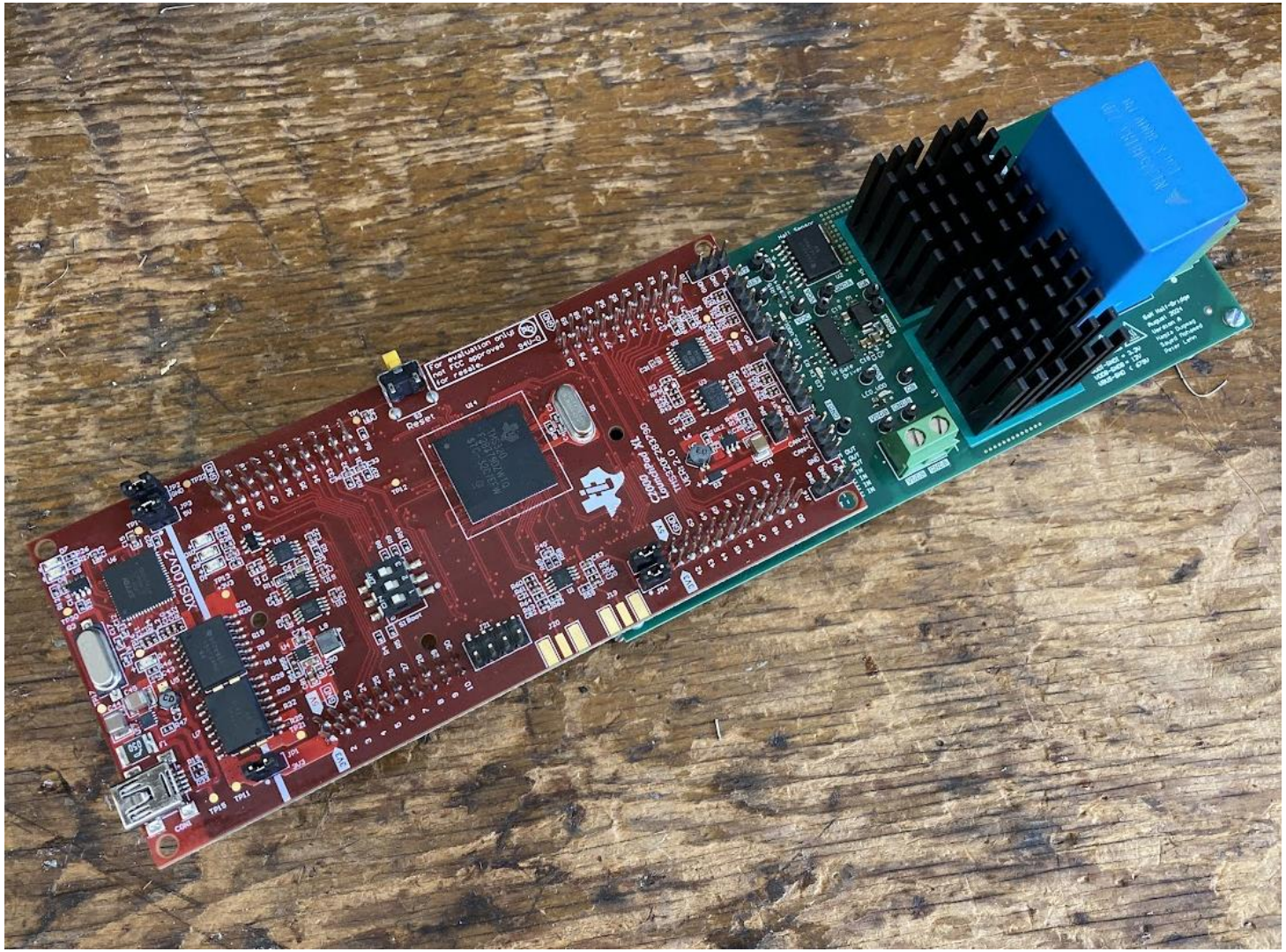
Agenda

1. Motivation
2. Switch Selection
3. Circuit Design
4. Simulations
5. PCB Design
6. Fabrication
7. Firmware
8. Testing
9. Conclusion



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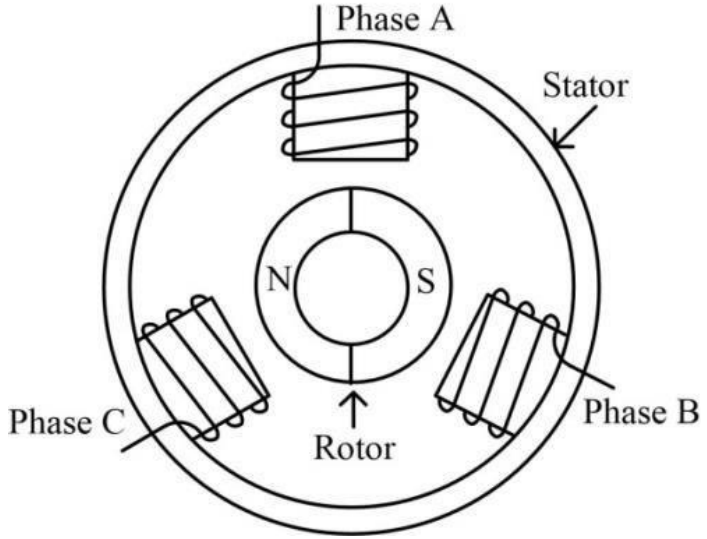
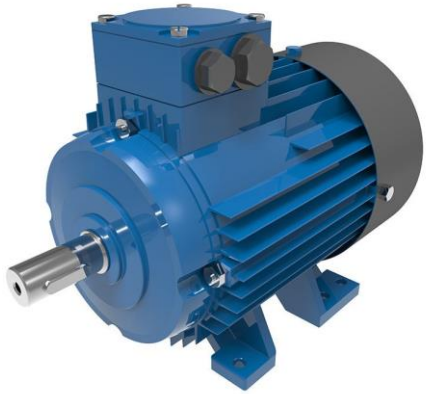
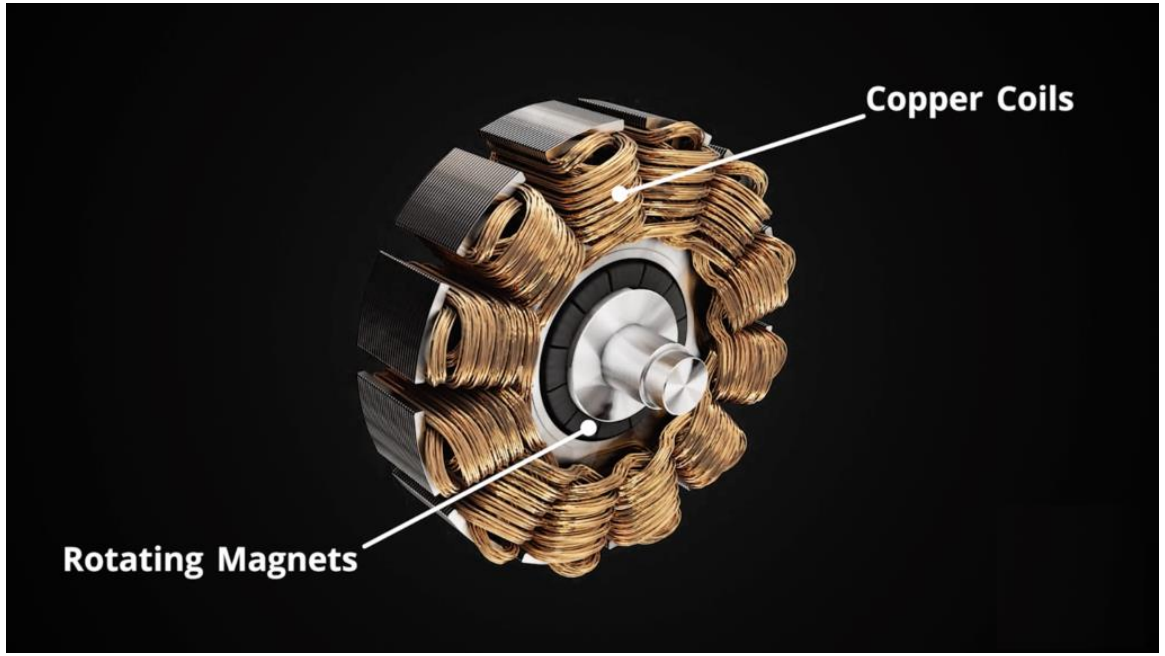
Motivation

Synchronous Motors (SM)



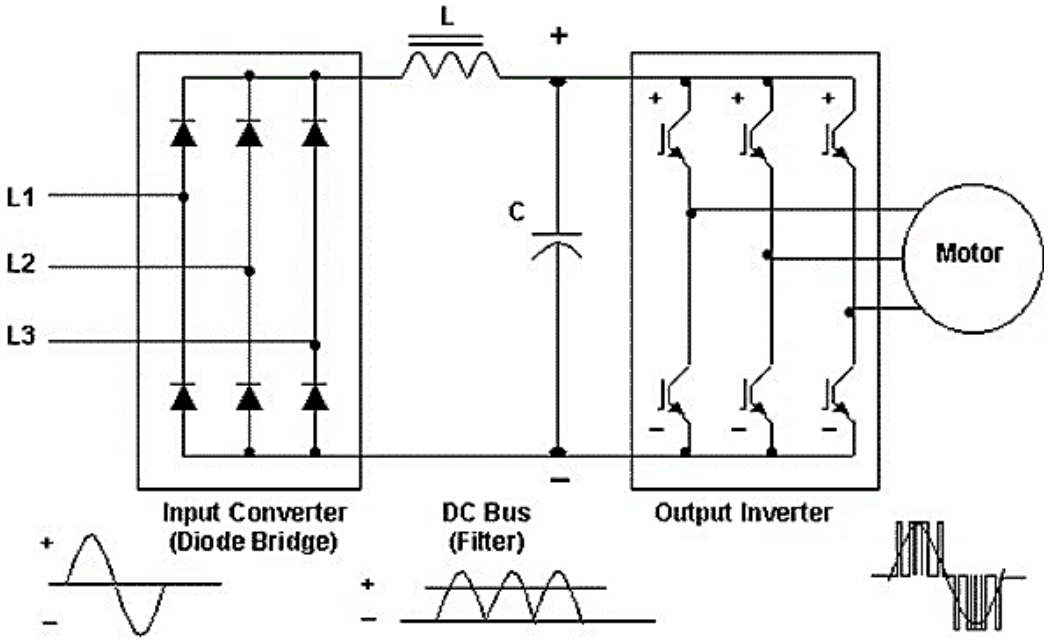
- Permanent magnet rotor → PMSMs
- Synchronous with stator magnetic field
  - Constant speed regardless of load
- Traditionally radial-flux
- Industrial applications
  - Pumps, fans, etc.

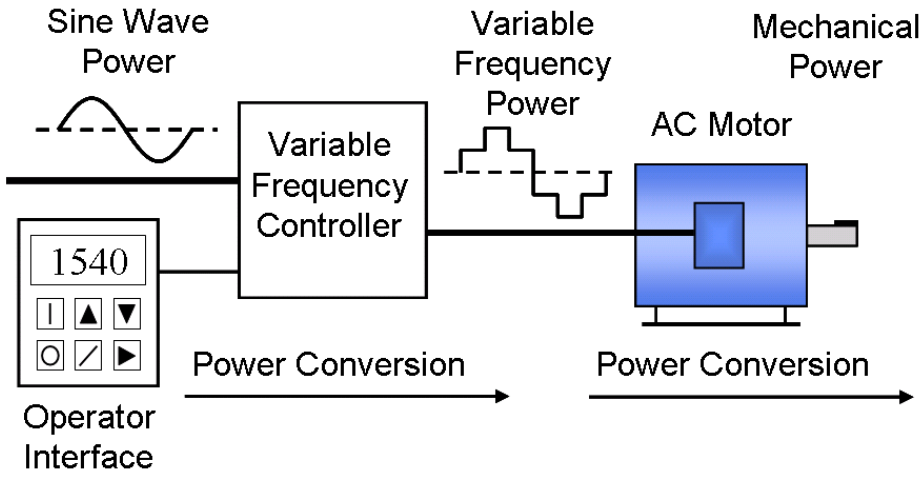




Variable Frequency Drive (VFD)

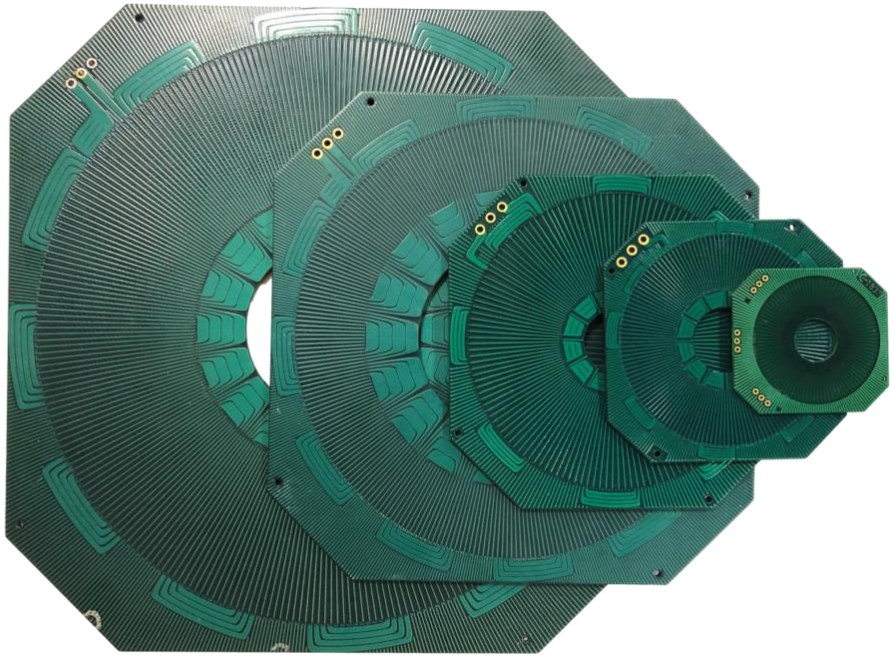
- Speed control → match energy demand
- AC (480VAC grid) → DC (679VDC) → AC (motor)

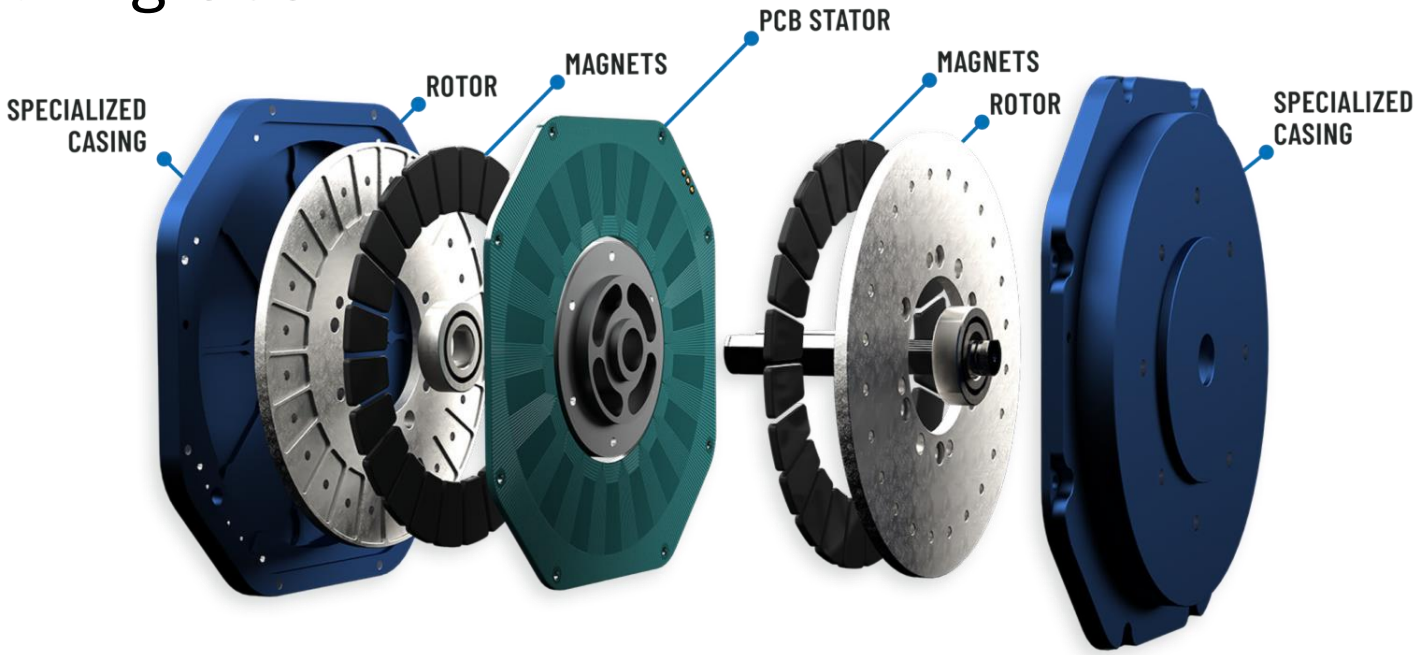




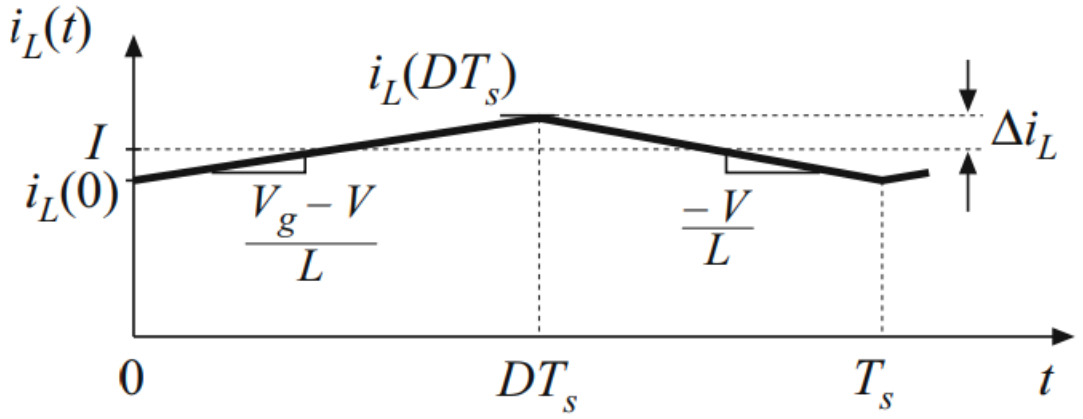
PCB-Stator PMSMs

- Axial flux
- ↑ Efficiency
- ↑ Power Density
- ↓ Manufacturing Cost

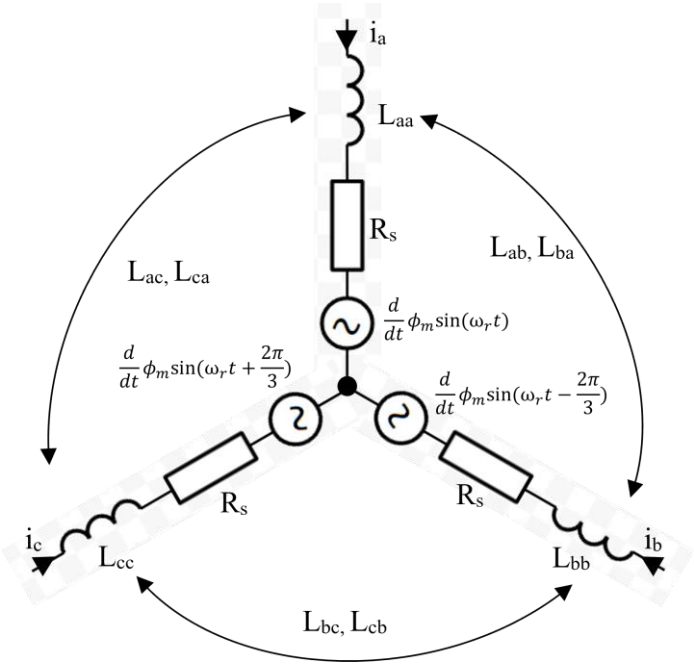


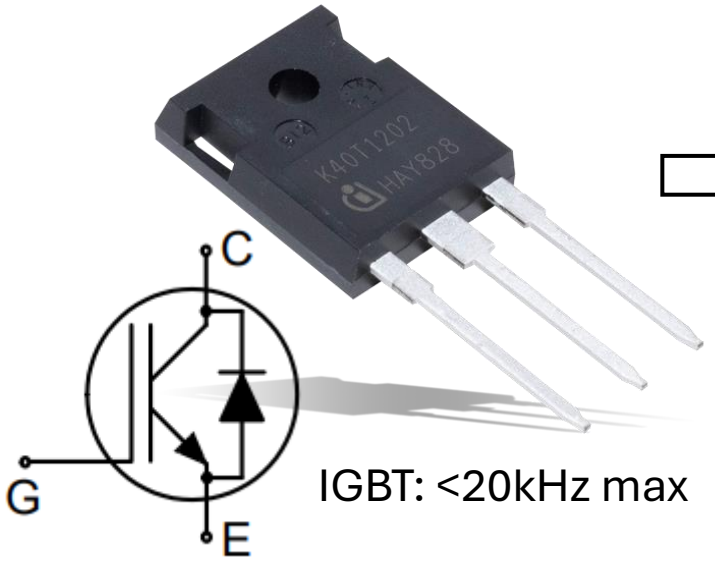


PCB-Stator



- Low stator inductance!
  - 10s of μH
- VFD switching frequency vs. filter size/weight/cost

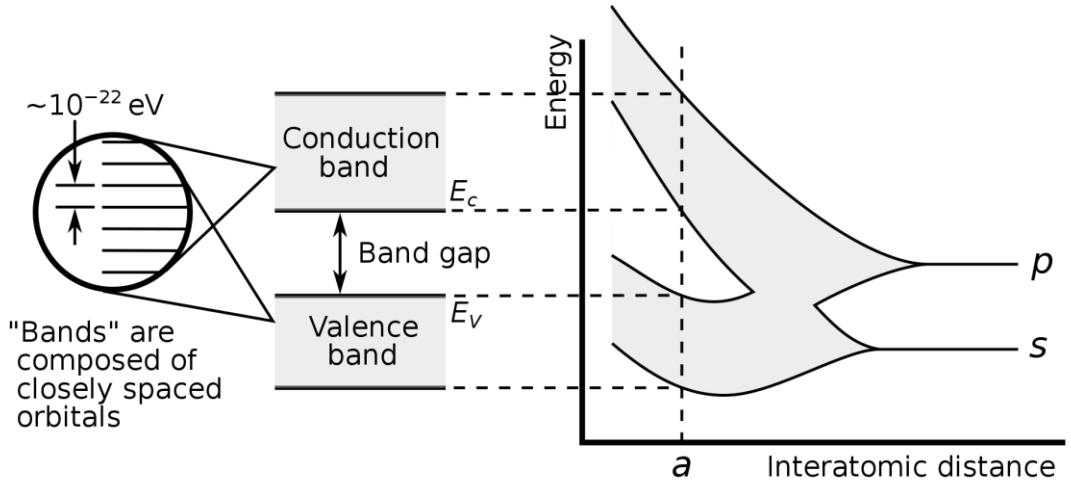




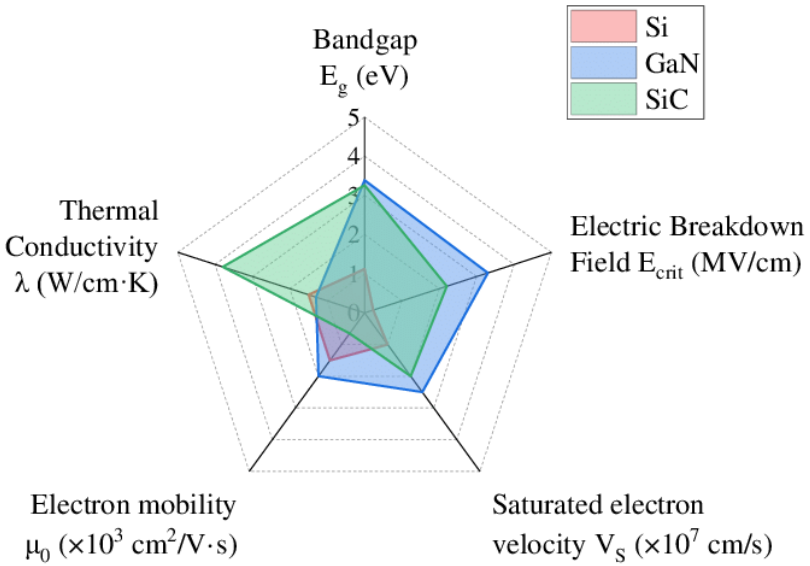
IGBT: <20kHz max

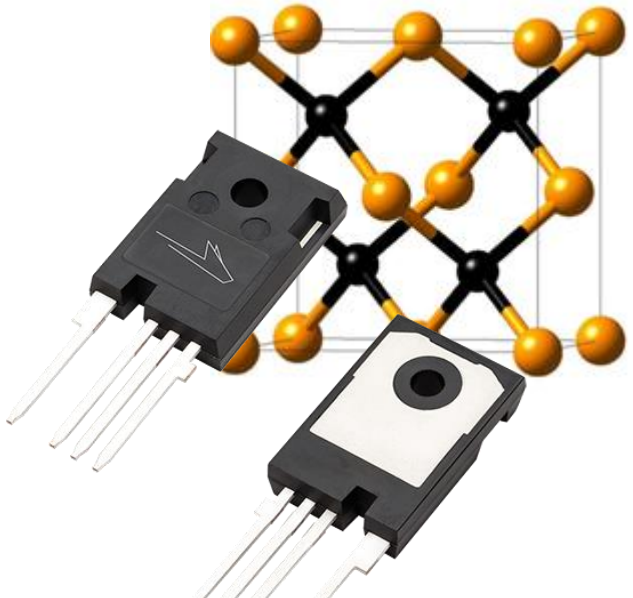
↑↑↑

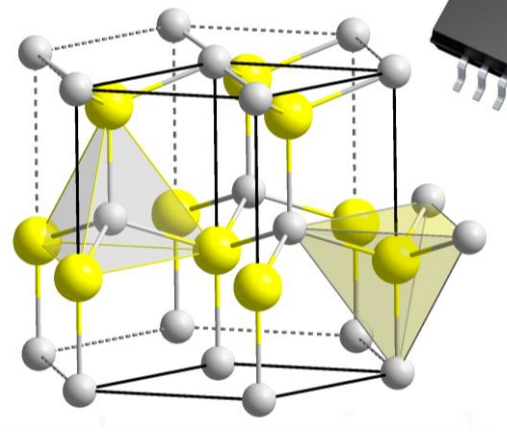
WBG Semiconductors



- **SiC**: 100s of kHz (↑↑ voltage)
- **GaN**: up to MHz! (↑↑ efficiency)
- High frequency, voltage, temperature applications
- Recently, GaN is showing ↑↑*V* and ↓$ → use in VFDs!







Project Objectives

- First step towards GaN-VFD for PCB-stator PMSMs
  - 2-year plan at LAPCSA
- Synchronous buck using **new** ultra high-voltage GaN switches
  - Open-loop SPWM (unidirectional half-bridge)
  - 679V
  - 3A
  - 200kHz
- Learn about GaN layout and driving techniques
- End-to-end ownership

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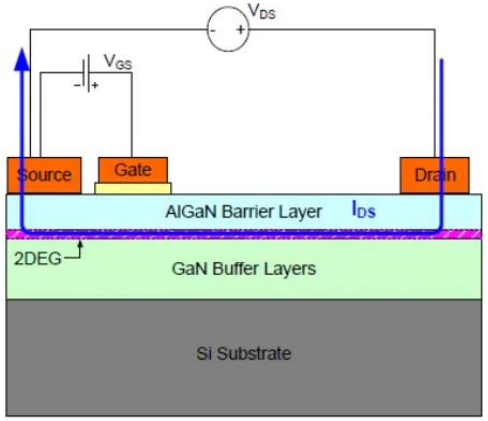
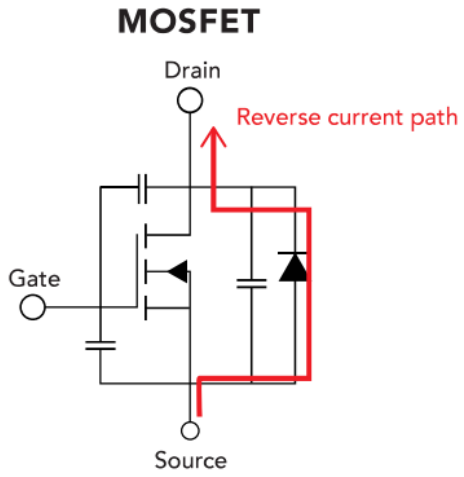
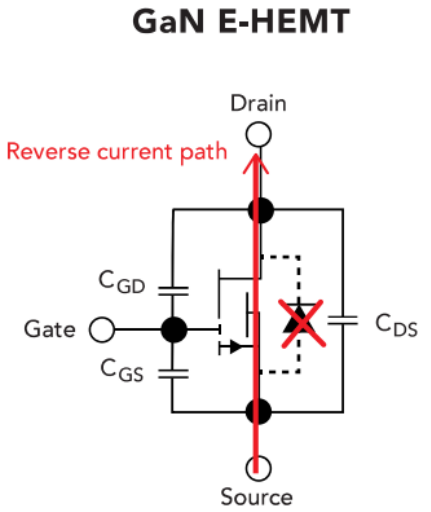
Switch Selection

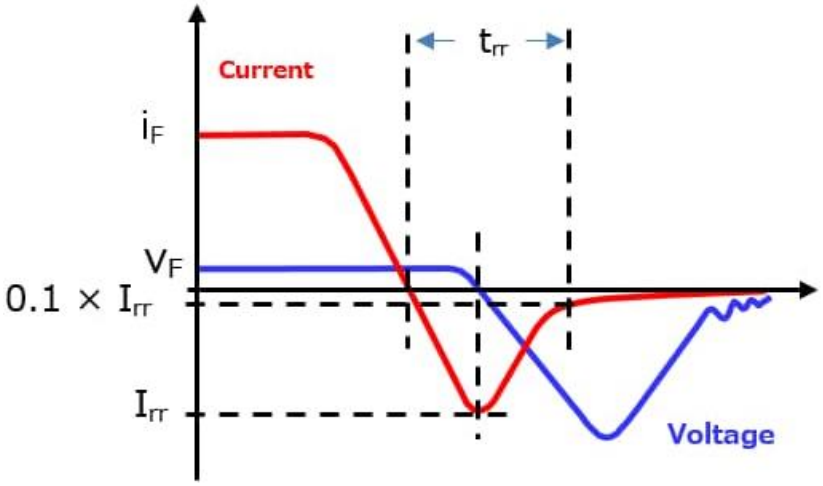
GaN Benefits

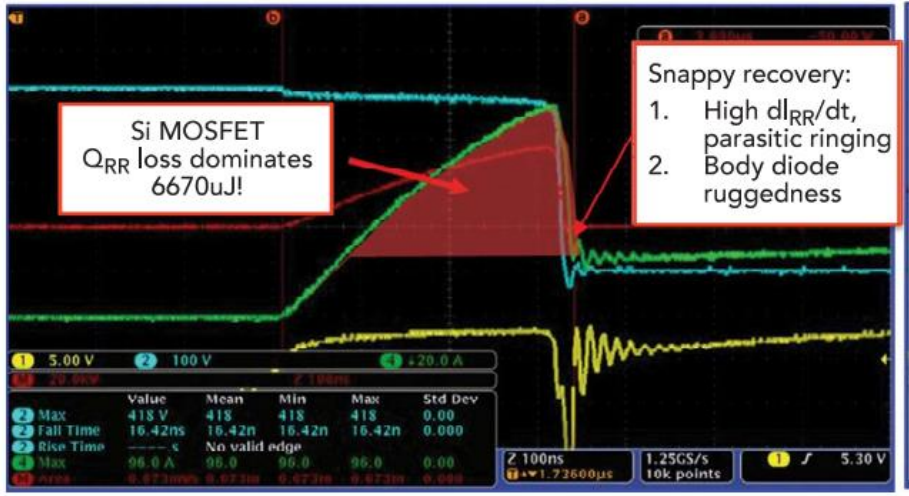
- ↓ $R_{ds,on}$ → ↓ P_{cond}
- ↓ Capacitances → ↓ P_{sw}
  - ↑ Switching speed and $f_{sw,max}$
- Effective body diode with $Q_{rr} = 0$

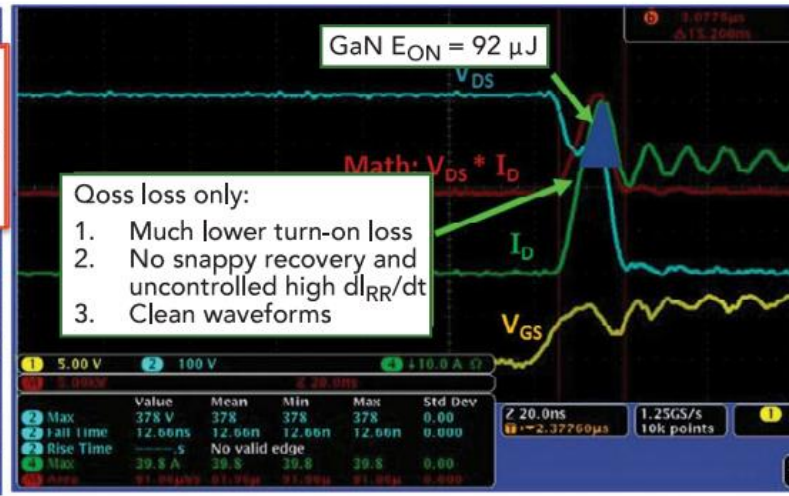






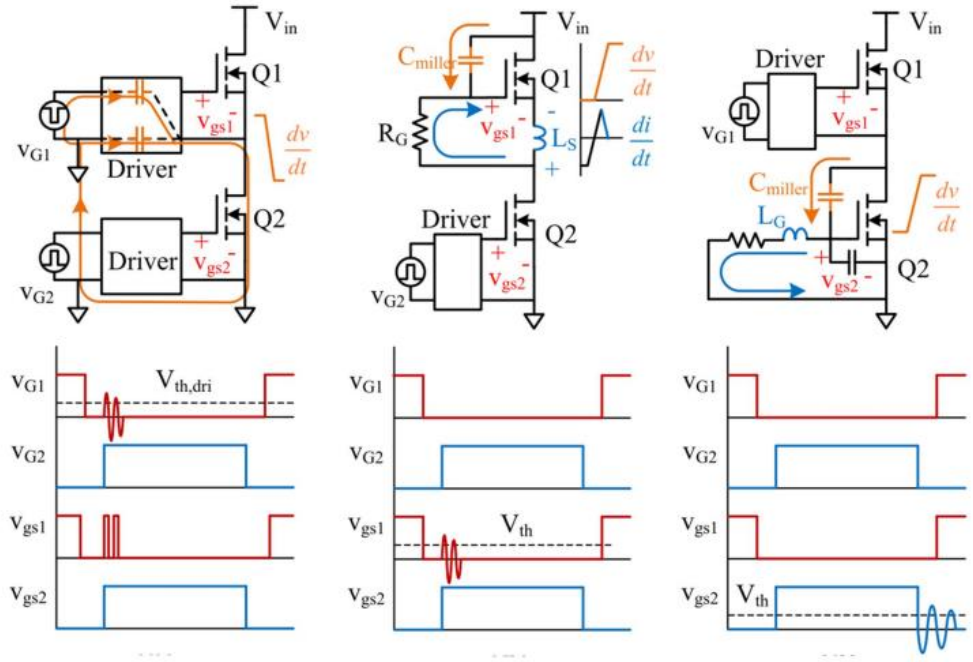






GaN Challenges

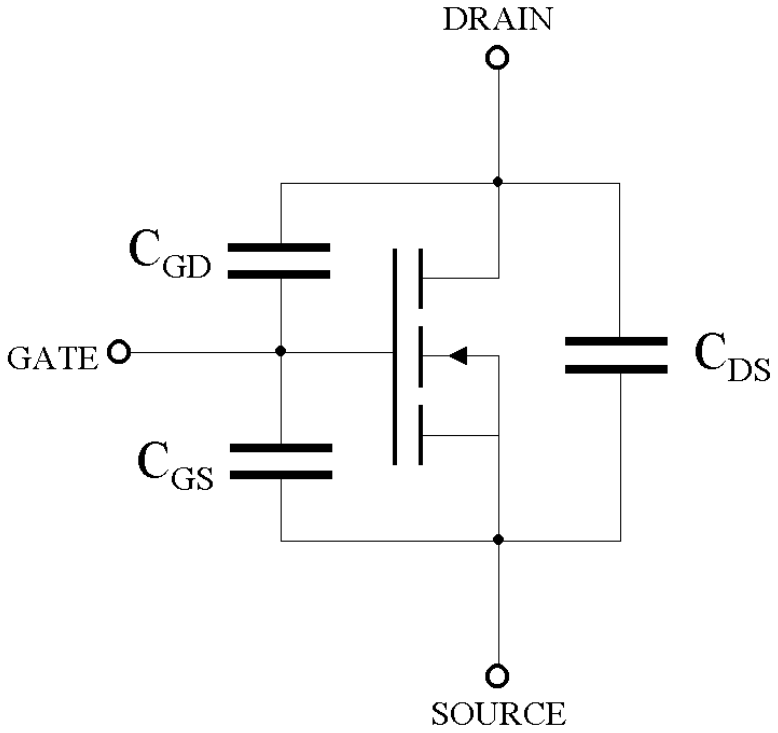
- ↑ *di/dt*
  - EMI generation
  - Parasitic inductance voltage spikes and ringing
- ↑ *dv/dt*
  - EMI generation
  - Parasitic capacitance leakage currents
  - Gate mis-triggering (↓ V_{th})
- Schottky gate → ↓ V_{gs} margin
- And more!

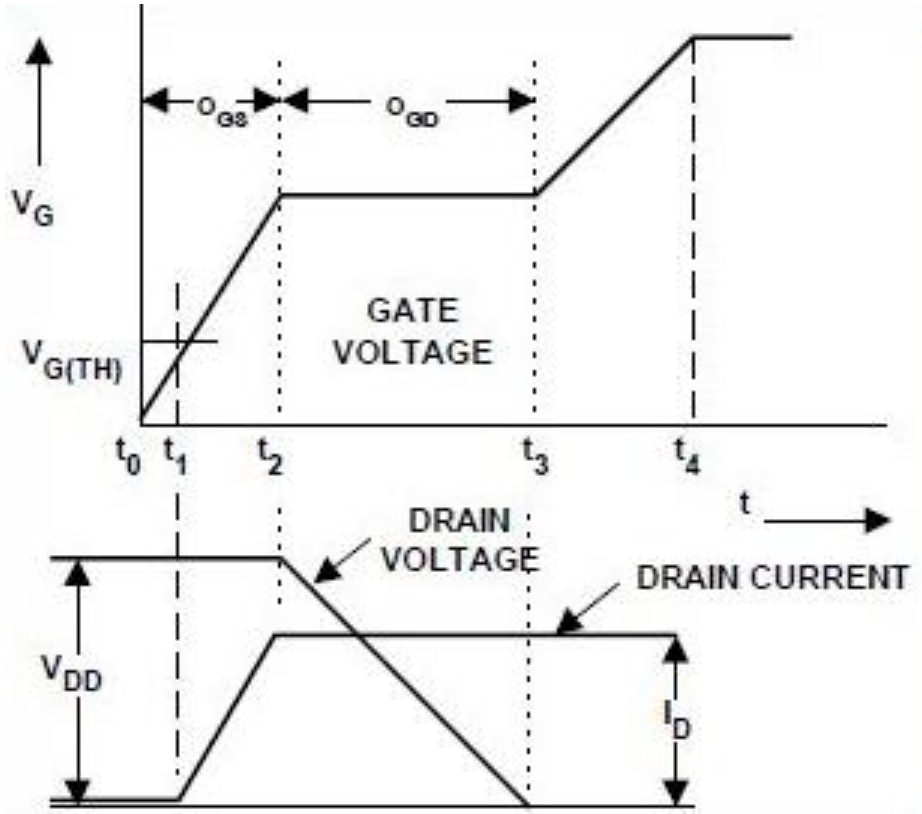


Ref.	Problem Statement	Root Cause	Solution
[101-106]	Voltage overshoot and oscillation in gate and power loop during switching action	Power loop and gate loop inductance	Reduction of loop inductance, slowing down switching action
[107-108]	Coupling of power and gate loop	Common source inductance	Use of kelvin connection
[109]	Coupling of power and gate loop	Coupling through mutual magnetic flux	Orthogonal placement of power and gate loop to reduce coupling
[110-114]	PWM distortion and subsequent mis-triggering	CM EMI noise due to high dV/dt, CM to DM noise transformation	Cascaded isolator stage in gate driver and EMI filter to reroute EMI noise
[115-121]	Mis-triggering of gate	Induced by leakage current from C_{gd}	Use of low gate resistance for turn off path, reduction of L_g
[123-125]	Dynamic current imbalance	Asymmetric power and gate loop, uneven heating of parallel die	Symmetric layout, Active gate driver solution
[126-128]	Coupling of power and gate loop in parallel device	Quasi common source inductance	Symmetric layout for power and gate loop, Unsynchronized gate driver
[129-130]	Circulating current in parallel device	Mismatch of input capacitance in paralleled device	Distributed gate resistance, diodes in gate loop of paralleled device
[131-133]	Sustained oscillation during reverse conduction	Instability due to the reverse conduction mechanism and feedback loop formed with circuit parasitic	Reduction of circuit parasitics, antiparallel diode across GaN transistors, RC snubber
[134-136]	Dynamic on resistance	Hot electron trapping under high electric field	Connection of the substrate to source potential to redistribute electric field
[137-141]	EMI induced compatibility problem	Impact of noise voltage source is shaped by the switching speed	Integrated EMI filter, reduction of stray capacitance from switching node

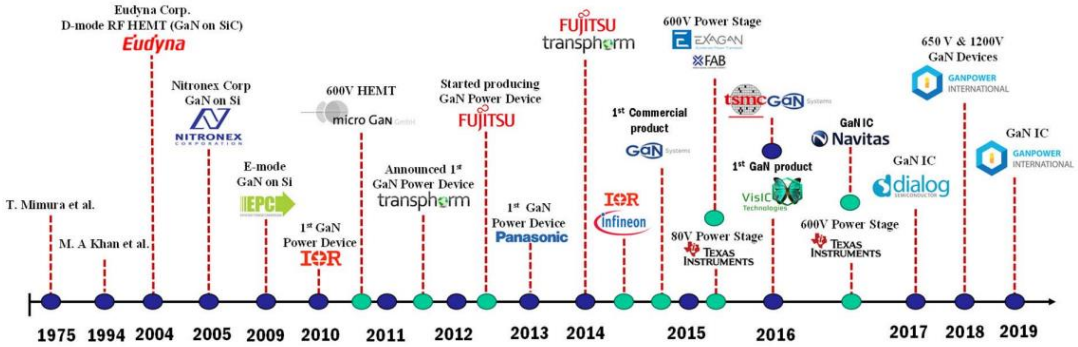
Miller Plateau

- C_{gd} charging interrupts C_{gs} charging
- ↑ P_{sw}
- ↑ I_g:
  - ↓ Miller time
  - ↑ EMI

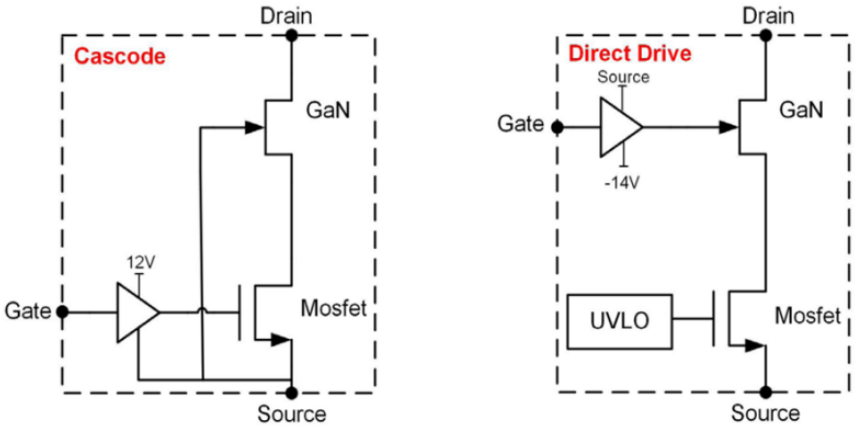




Market Study



- Mostly 650V devices… (<679V×FOS)
- Two suppliers of 900/1200V GaN
  - **Enhancement Mode:** *IGaNPower*
    - Nominally off: $V_{th} > 0$
  - **Depletion Mode:** *Transphorm*
    - Nominally on: $V_{th} < 0$
    - Techniques for nominally off:

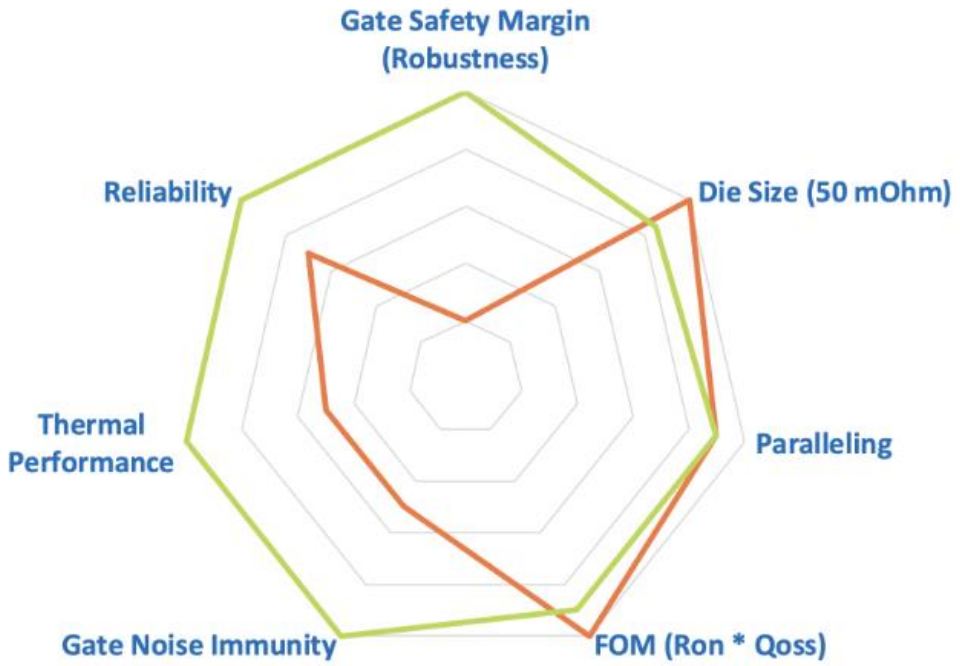


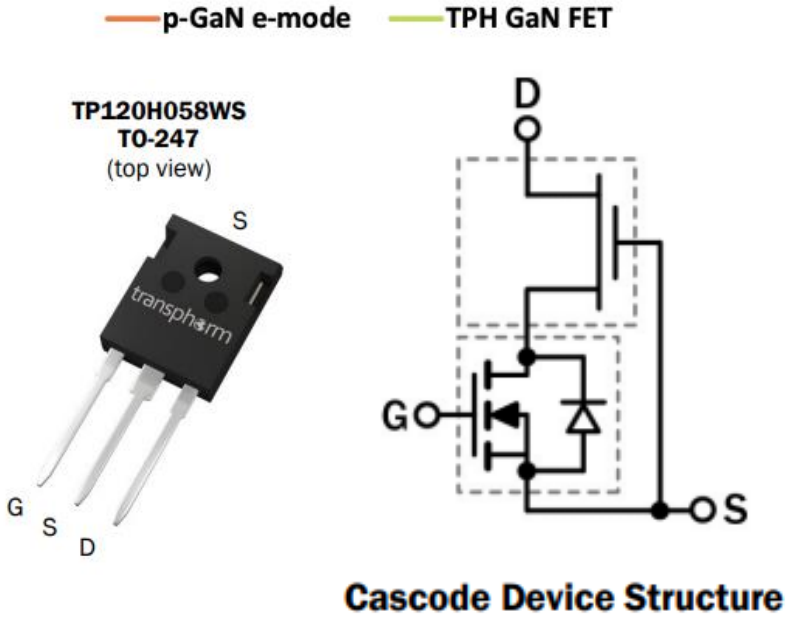
GANPOWER INTERNATIONAL

transphorm

D-Mode Cascode

- More robust
  - Partly from ↑ V_{th}
- Low-voltage series Si MOSFET:
  - ↑ $R_{ds,on}$ → ↑ P_{cond}
  - $Q_{rr} > 0$
  - ↑ Capacitances → ↑ P_{sw}
    - ↓ Switching speed and $f_{sw,max}$





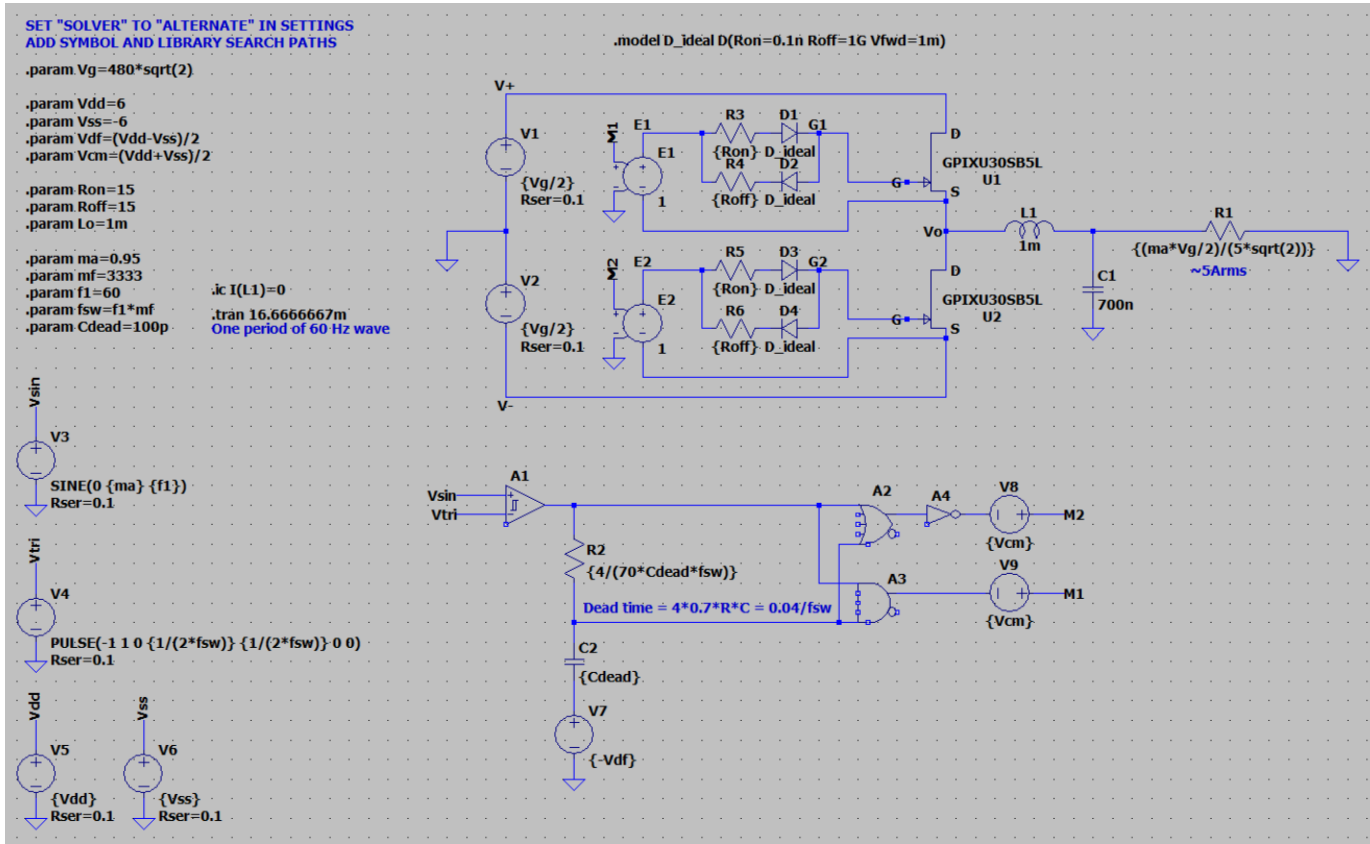
Technology Comparison

- Hypothesis: **eGaN > dGaN > SiC**
  - Speed and losses
- Compare devices with similar BV_{DSS}, package (layout and cooling), junction size:
  - $I_{ds,max}$ = ~30 A
  - $R_{ds,on}$ = ~50 mΩ
  - T_{max} = ~150 °C
- Simulate in *LTspice*

Comparative Simulation

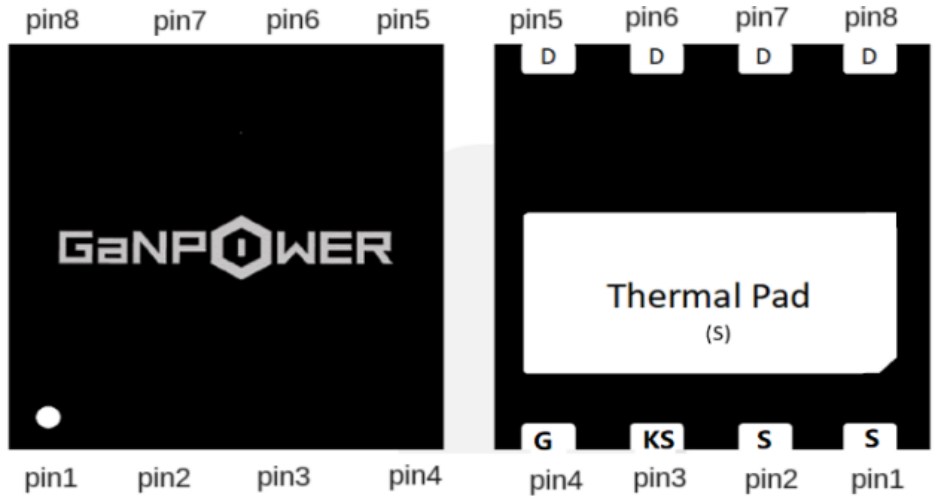
- Investigate hard-switching
  - Ideal half-bridge, LC filter, R load
  - Ideal driving, SPWM
  - $V_{gs,op}$ [V] and R_g [Ω] from datasheet/application notes
- Efficiency results:
  - **eGaN: ~99%**
  - dGaN: ~96%
  - SiC: ~98%

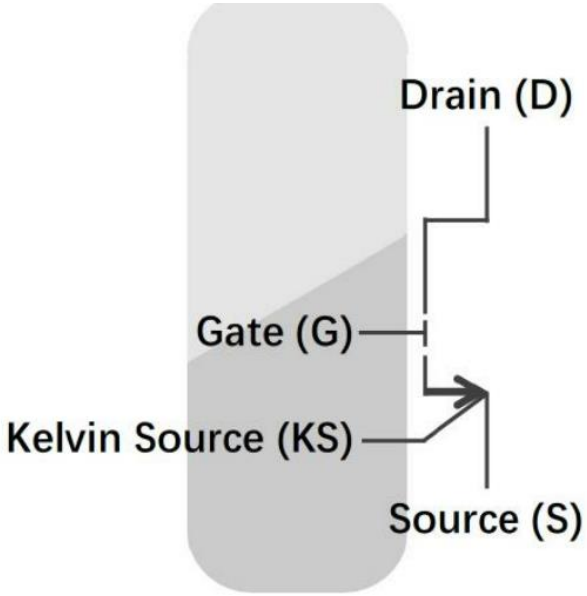
Circuit Parameters	
Toperate [°C]	25
Vdc [V]	678.82
ma	0.95
mf	3333
f1 [Hz]	60
fsw [Hz]	199980
tdead [ns]	200.02
Lo [mH]	1
Co [nF]	700
Ro [Ohm]	45.6

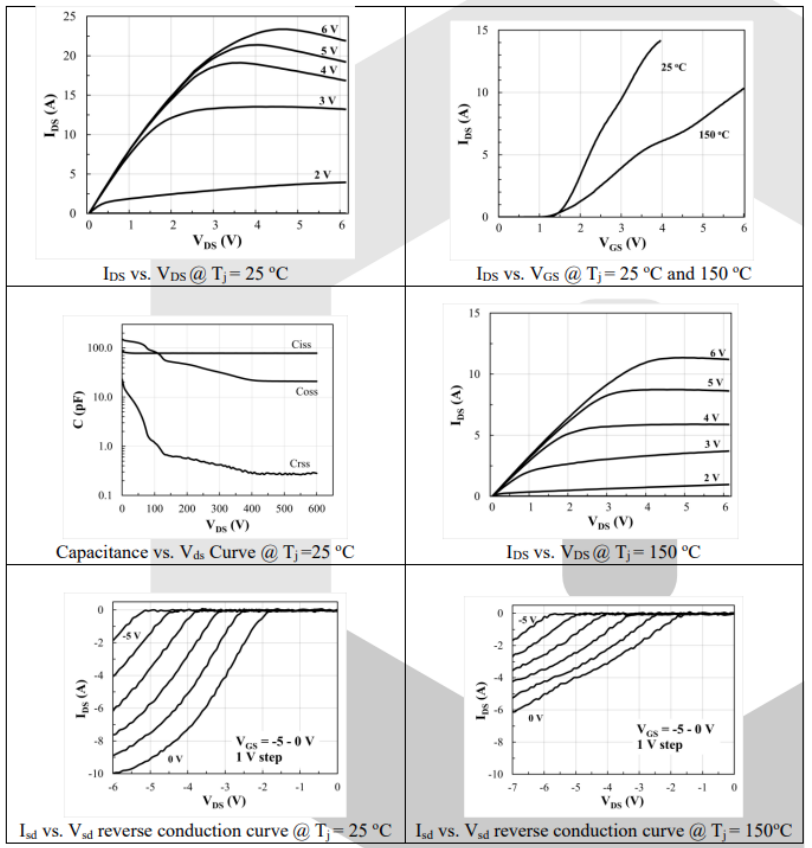


Switch Selection

- 1200V 30A *IGaNPower* out of stock…
- Try 900V 10A:
  - Will get similar learning experience
- **GPI90010DF88:**
  - DFN8x8 package (↓ L_{lead})
  - BV_{DSS} = 900 V
  - $I_{ds,max}$ = 10 A
  - $R_{ds,on}$ = 120 mΩ
  - Bottom-cooled







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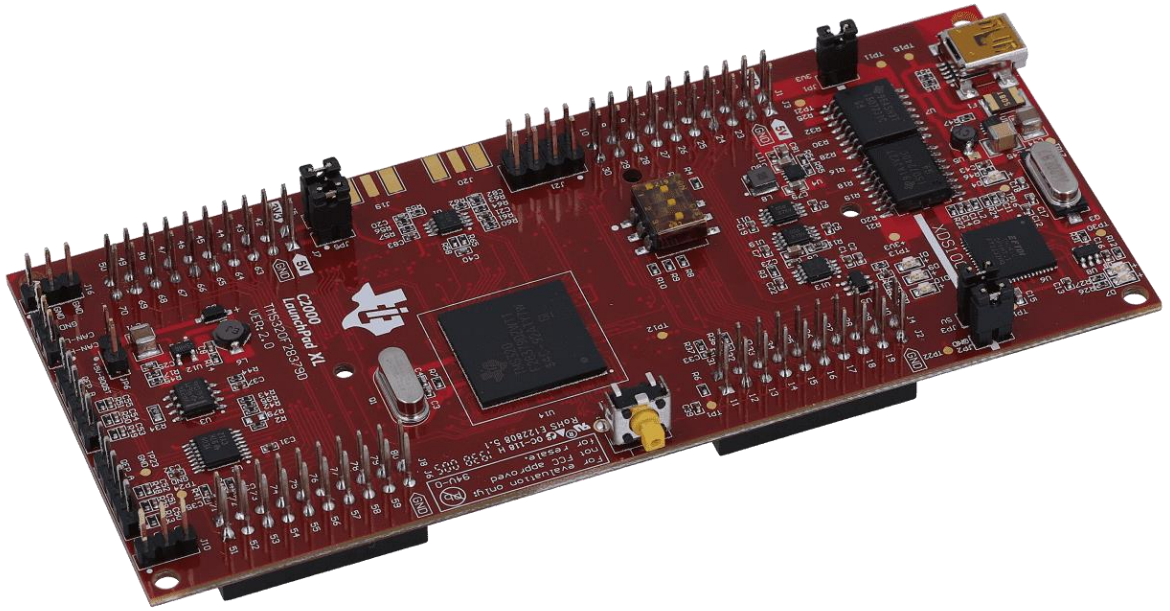
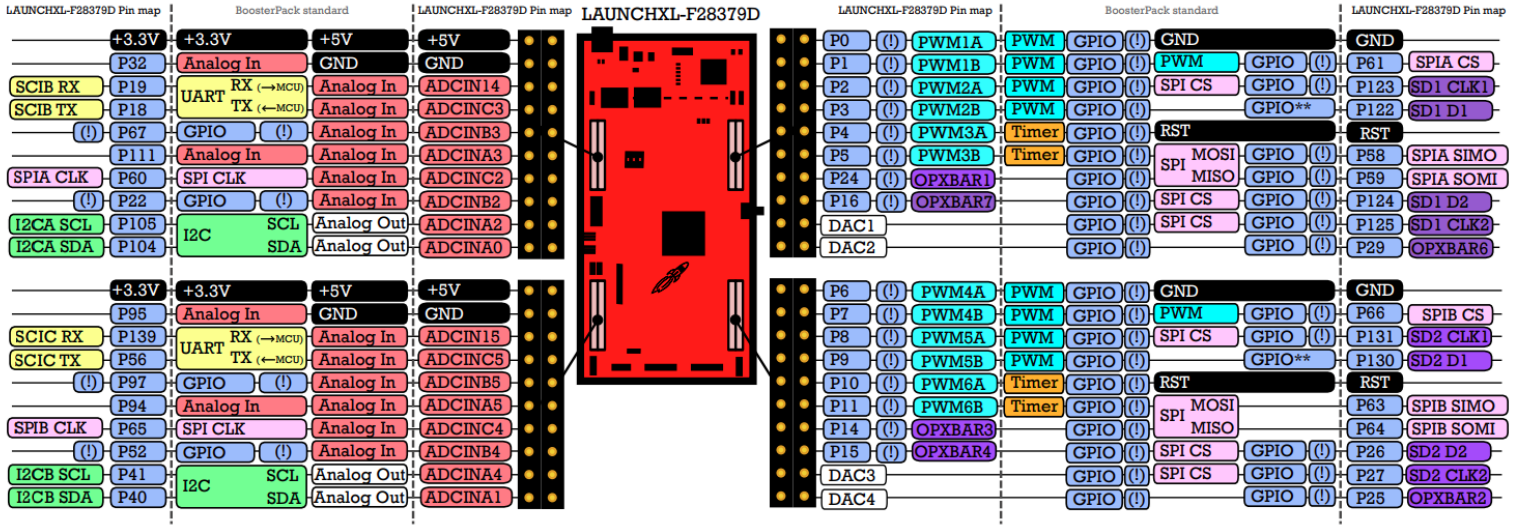
Circuit Design

Microcontroller

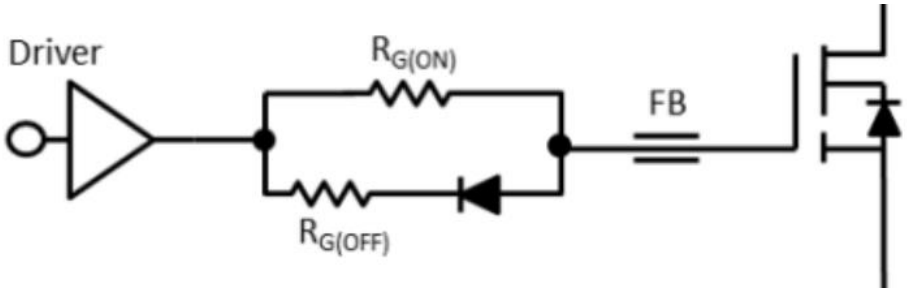
- **TI F28379D LaunchPad (C2000):**
  - Isolated USB
  - 3.3 V
  - 12/16-bit ADCs
  - High resolution PWM:
    - Complementary channels
    - Dead time support
    - 100 MHz resolution





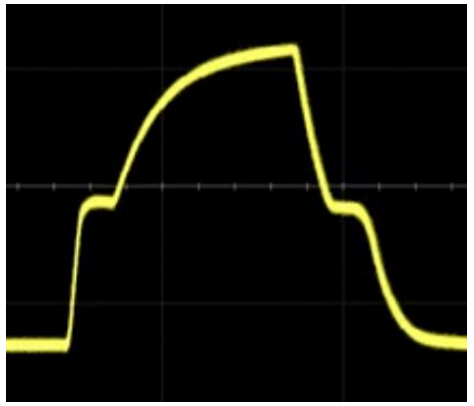
Gate Resistors

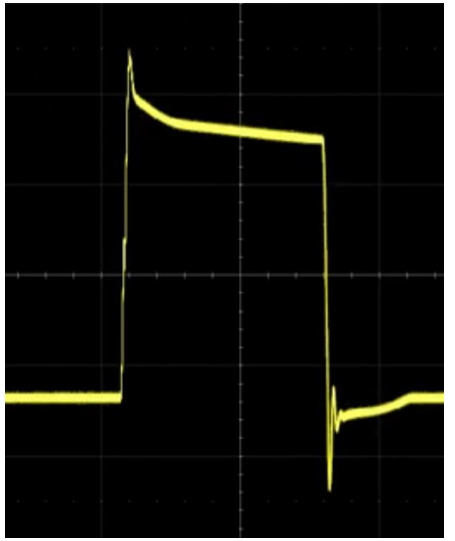
$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$



$$R_{GATE,OPT} = 2 \times \sqrt{\frac{L_S}{C_{ISS}}} - (R_{DRV} + R_{G,I})$$

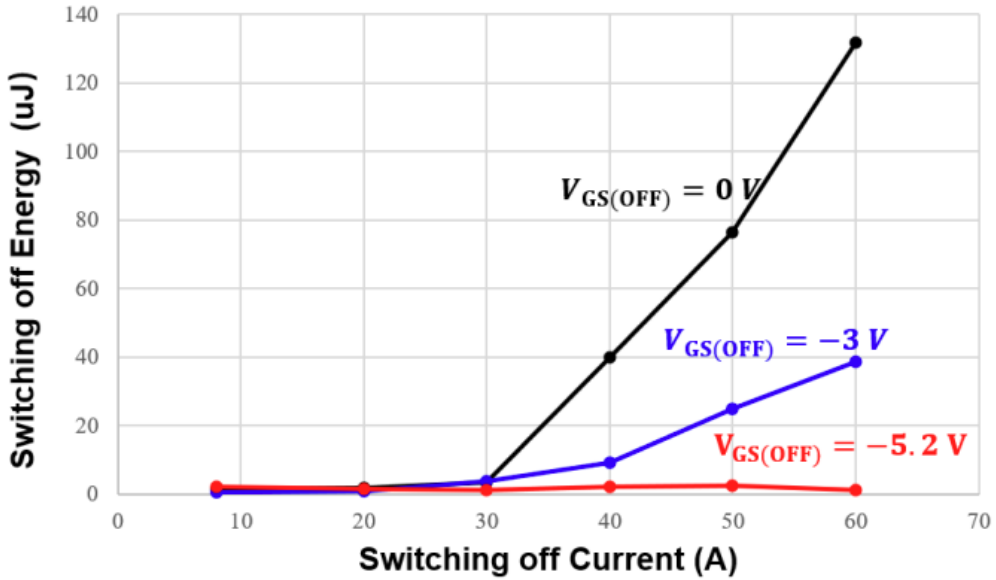
- Control C_{gs} (dis)charging
- $R_{off} < R_{on}$
  - Guarantee turn-off before turn-on of other side (avoid shoot-through)
  - ↓ Miller turn-on
- Trade-offs with ↑ R:
  - Pros: ↓ EMI and ringing, ↓ Gate driver power
  - Cons: ↓ Switching speed and ↑ Miller plateau → ↑ P_{sw}
- Optimized in simulation
  - Difficult to calculate analytically
  - Expect on the order of 5-30Ω
  - Want slight underdamping



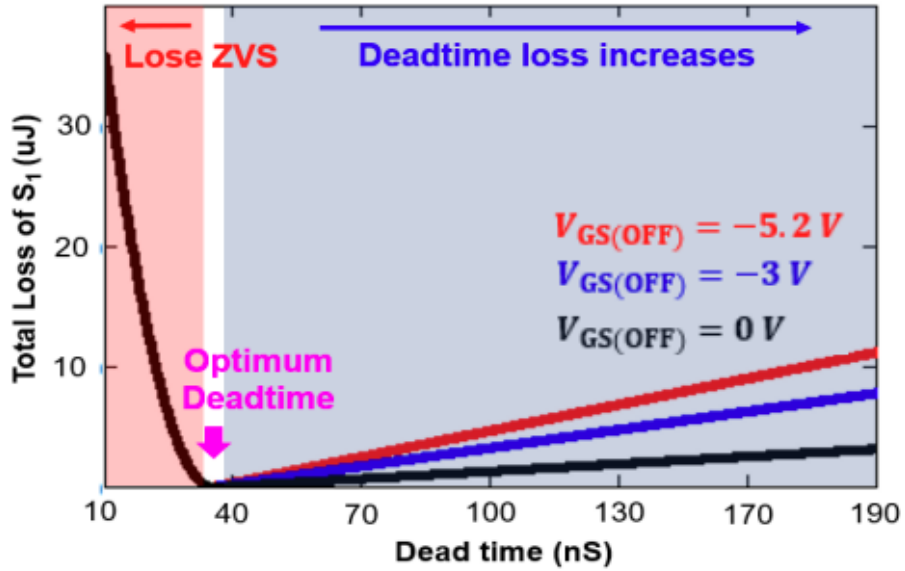


Negative-Voltage Turn-Off

- Pros:
  - ↑ Noise immunity
    - Recall ↓ V_{th}
  - ↓ Switching-off loss
- Cons:
  - ↑ Dead-time loss
  - Difficult implementation
- Pros + other GaN benefits outweigh cons

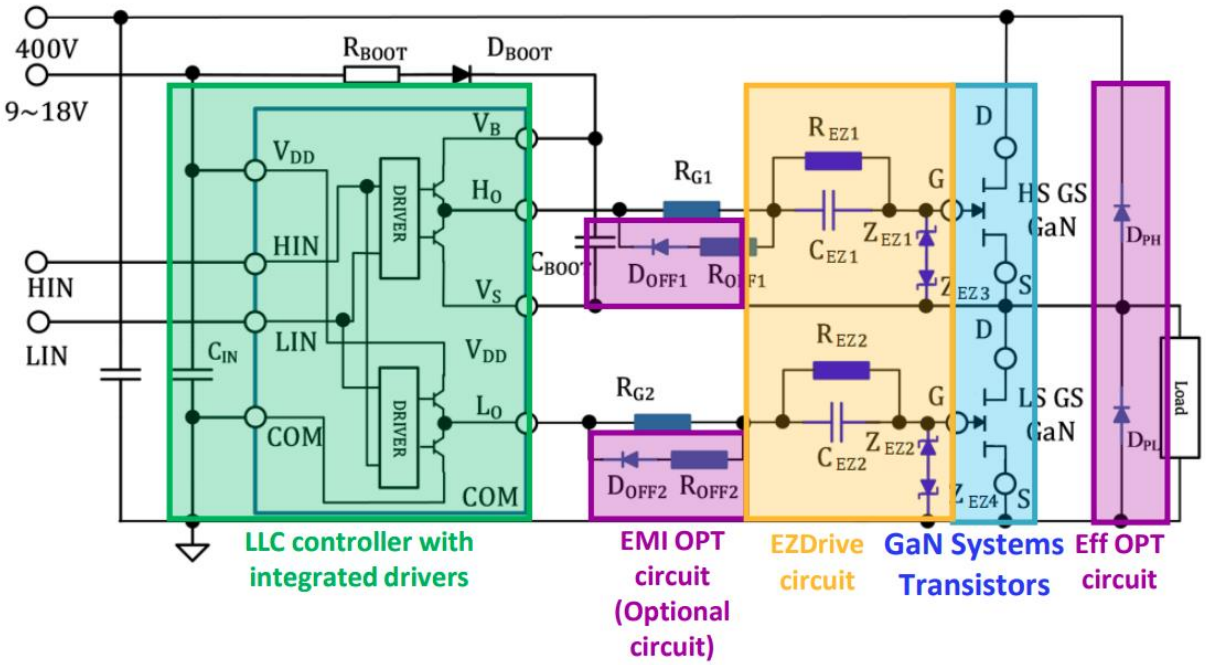


Switching-off loss of GS66516B vs. current at V_{BUS}=400 V, 25°C, R_G=1Ω



Level-Shifting

- Gate drivers output >0V… Clamp with Zener diodes!
- Cheaper and simpler than digital isolator + non-isolated driver
- Recommended by *IGaNPower*, *GaNSystems*, and *Nexperia*



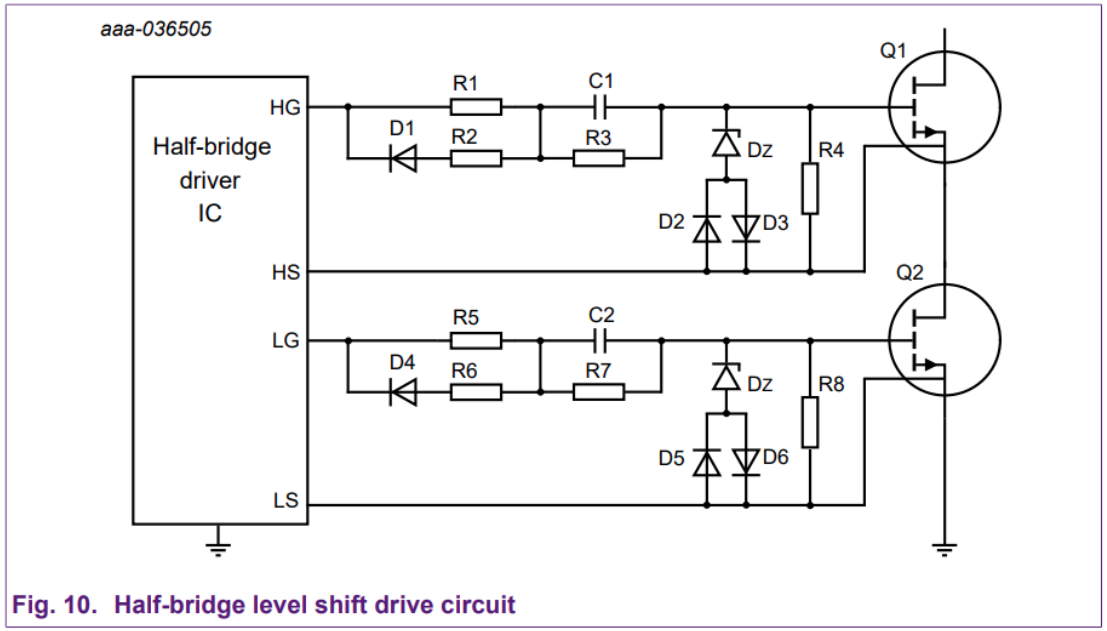
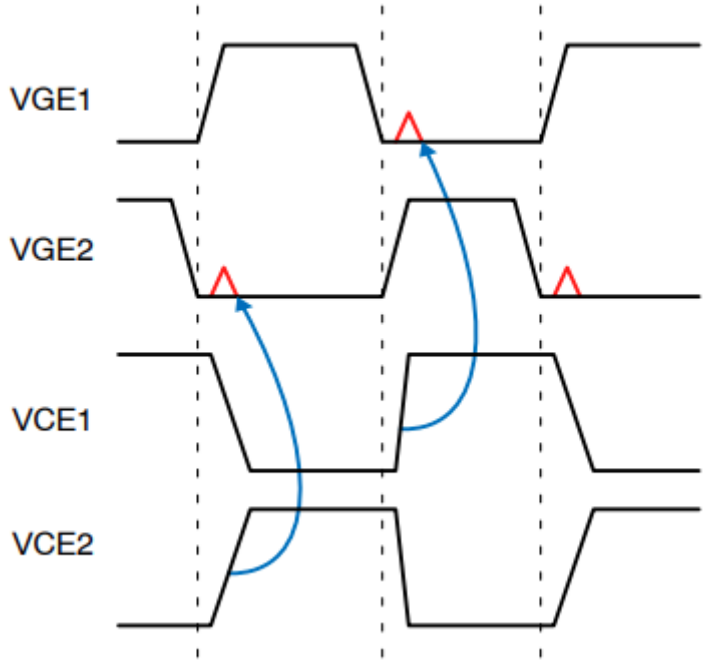


Fig. 10. Half-bridge level shift drive circuit

Miller Clamp

- Stabilize turn-on voltage → ↓ Overdriving risk
- Mitigate parasitic Miller turn-on from ↑ *dv/dt*
  - C_{gd} tries to pull up V_{gs}
- Zener diodes act as passive Miller clamp
  - Low impedance path for C_{gd}



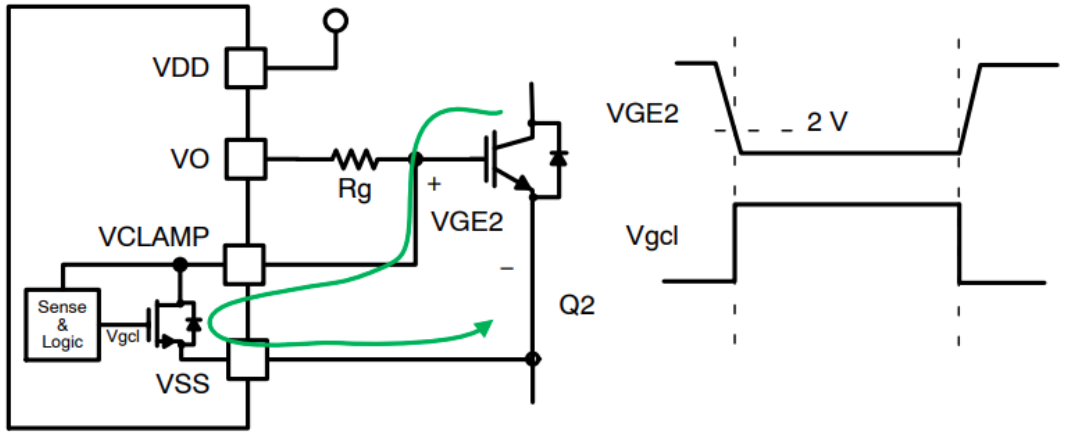
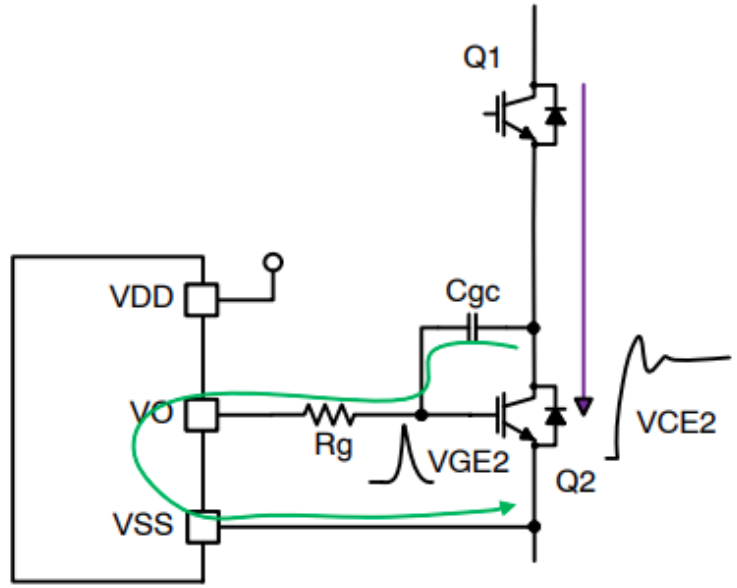
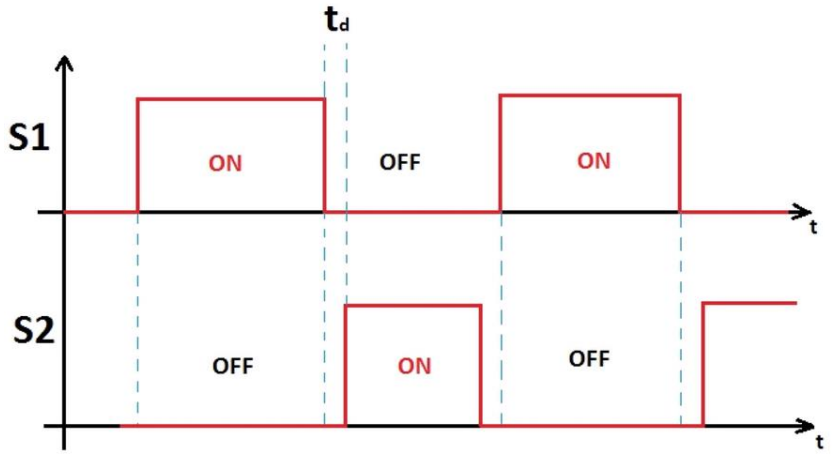


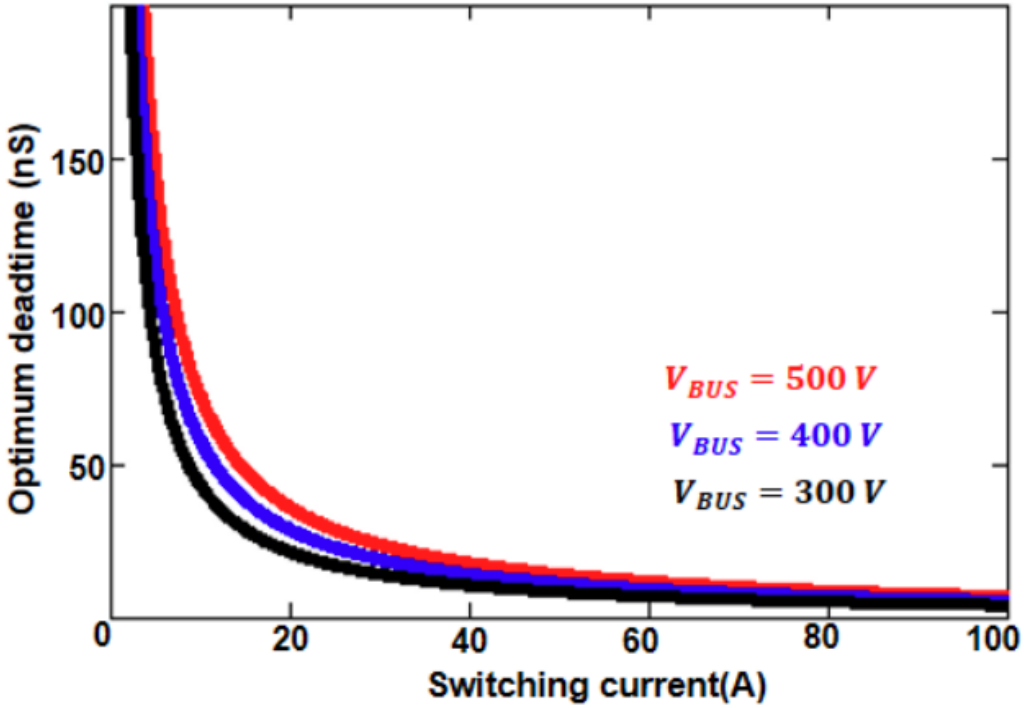
Figure 6. Active Miller Clamp Technology



Dead-Time



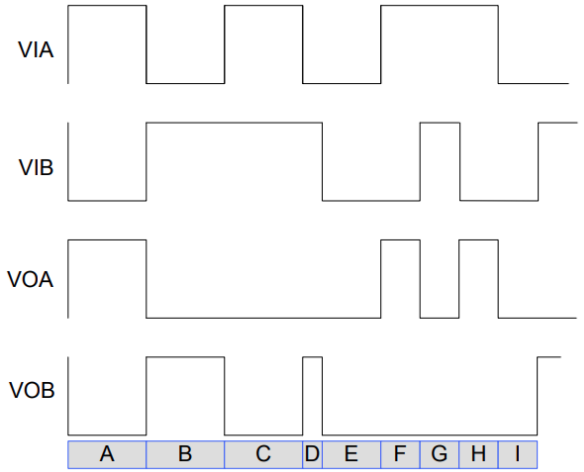
- Prevent shoot-through
- Limited by DSP's PWM resolution: 100MHz → 10ns
- Rule of thumb: 1% of T_{sw}
  - 0.01/200k = 50ns
- Testing at <5A:
  - Low V_{bus}: ~50ns
  - Nominal V_{bus}: ~200ns

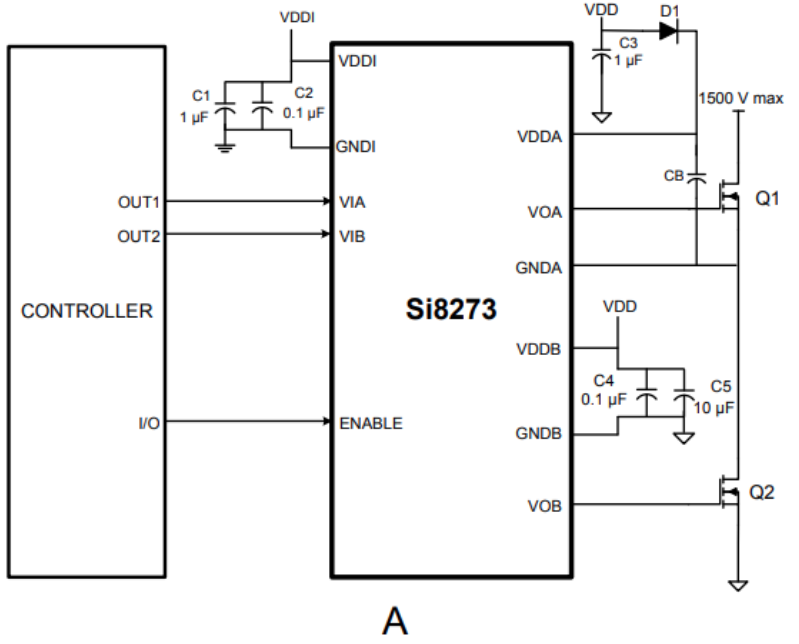


Gate Driver

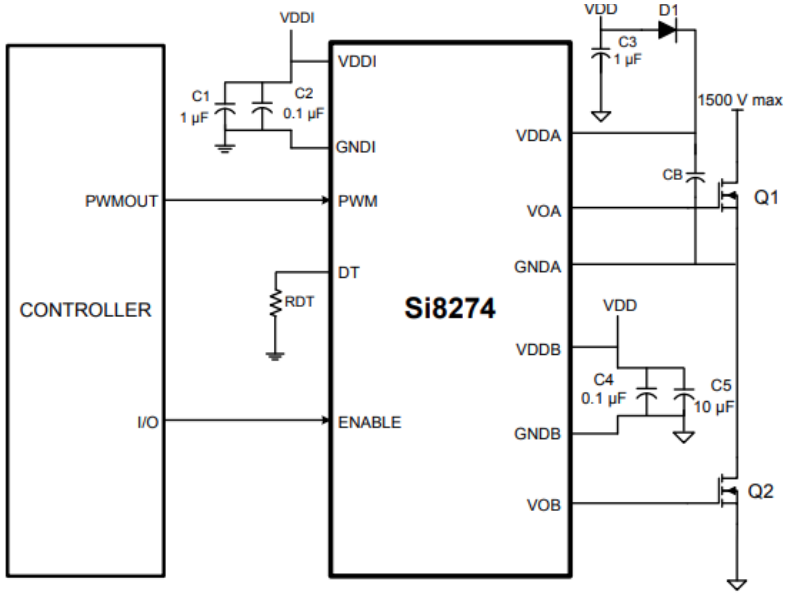
Gate Drivers		Configuration	Isolation	Notes
SILICON LABS	Si8271	Single switch	Isolated	Split outputs
	Si8273/4/5	Half-Bridge	Isolated	Dead time programmability
ANALOG DEVICES	ADuM4121ARIZ	Single Switch	Isolated	Internal miller clamp
BROADCOM	ACPL-P346	Single Switch	Isolated	Internal miller clamp
HEYDAY	HEY1011	Single Switch	Isolated	Power Rail Integrated
ON Semiconductor	NCP51820	Half Bridge	Non-Isolated	Bootstrap voltage management
RENESAS	RAA226110	Single Switch	Non-Isolated	Programmable Source Current and Adjustable Overcurrent Protection

- **Silicon Labs Si8273:**
  - Recommended by many GaN suppliers
  - High CMTI (200 kV/µs)
  - Isolation (semiconductor-based)
  - Half-bridge driver → easy implementation
  - <1500 V bus
  - Overlap protection
- Si8274: hard to change DT





A



B

Bootstrapping

- Floating high-side source!
- D_B:
  - Minimize recovery time
  - Reverse-block full bus voltage
- C_B: Design for ripple (avoid UVLO) and refresh time
- R_B: Design to minimize inrush current on startup

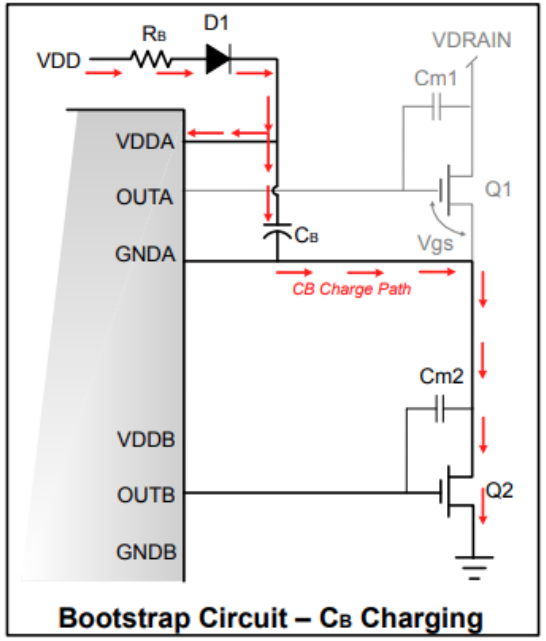


Figure 1.1. Bootstrap Circuit—C_B Charging

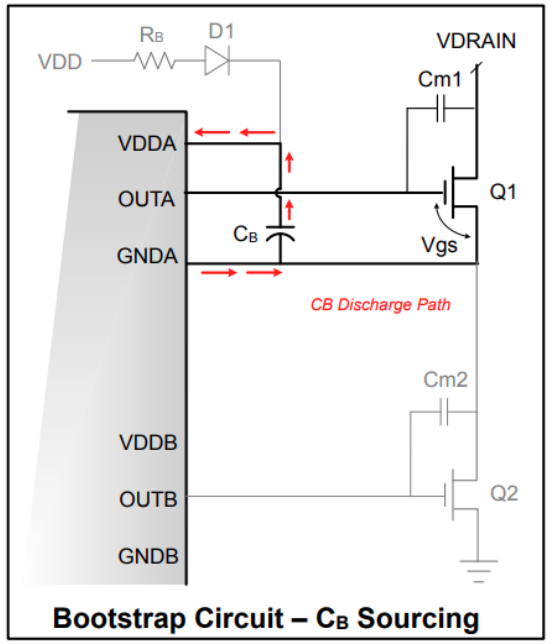
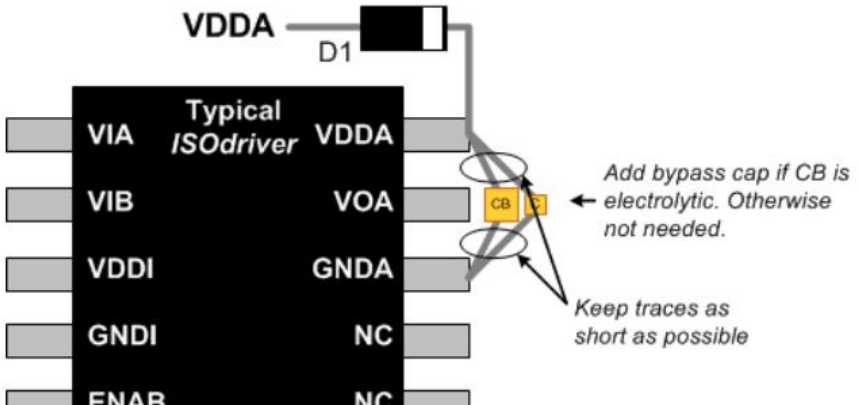


Figure 1.2. Bootstrap Circuit—C_B Sourcing

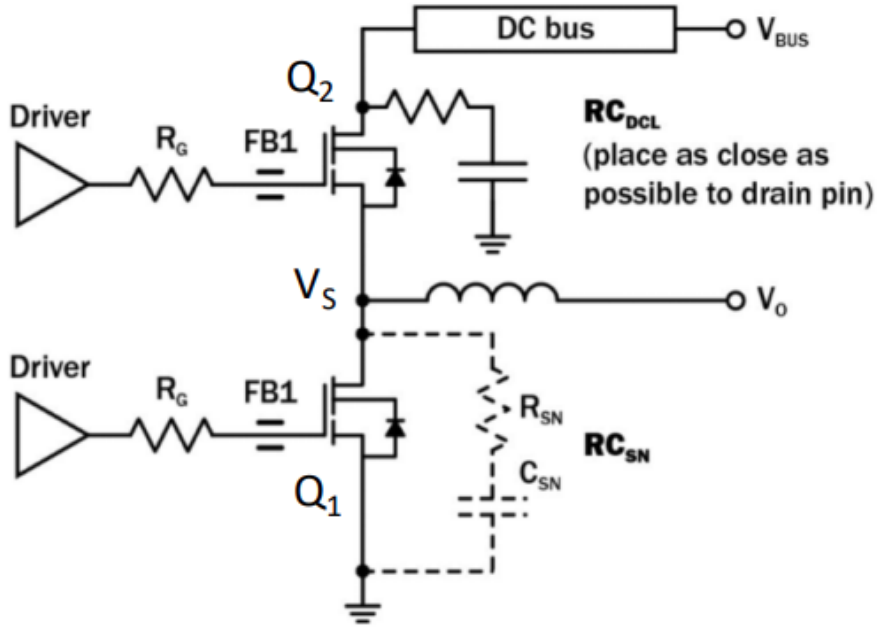


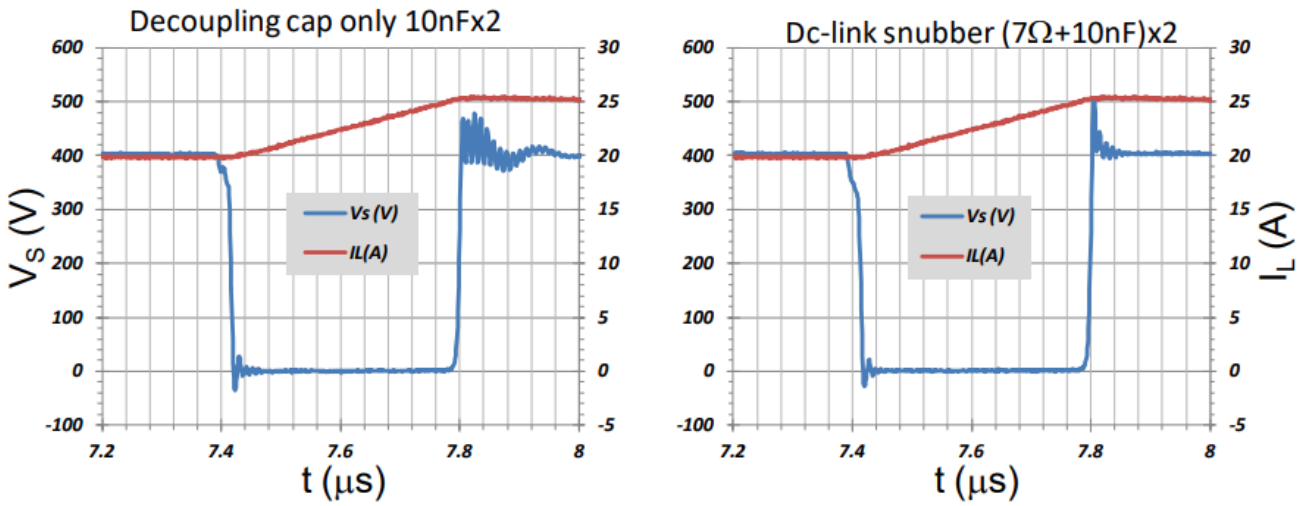
$$Q_{CB} = Q_G + (t_{Lmax} \times I_B)$$

$$C_B \geq \frac{Q_{CB}}{\Delta V_{CB}}$$

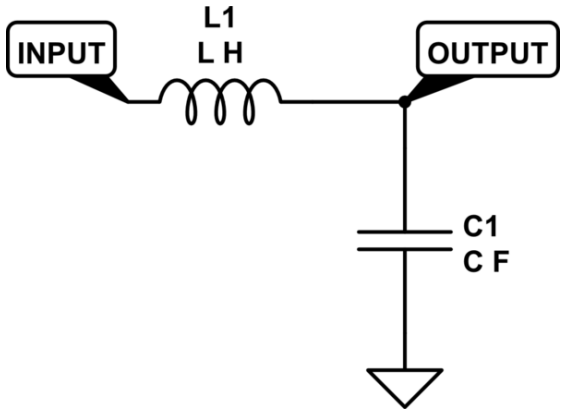
RC Snubber

- Cheap, simple, popular
- Protect against voltage transients:
  - ↓ Spikes and oscillations
  - ↑ Lifespan and ↓ EMI
- $C_{sn} > C_{oss}$: low impedance path
- R_{sn}: additional damping and dissipate power externally
- Design process:
  - Refer to application notes
  - Optimize in simulation

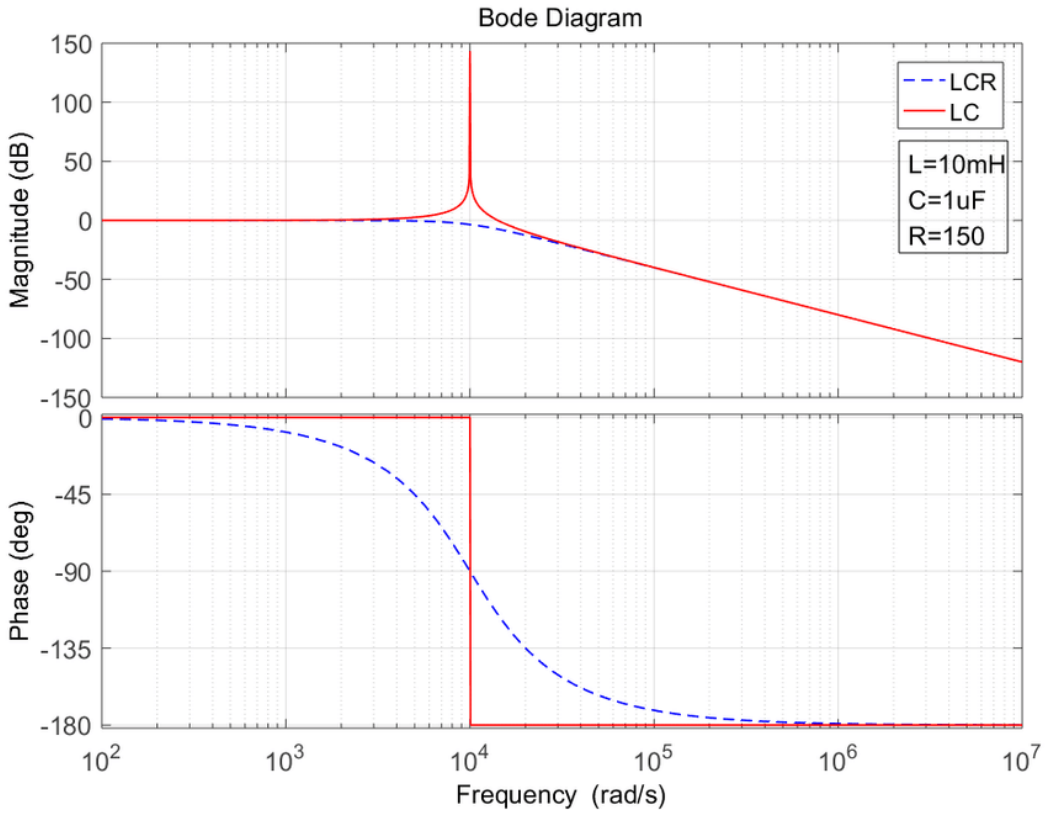




LC Filter

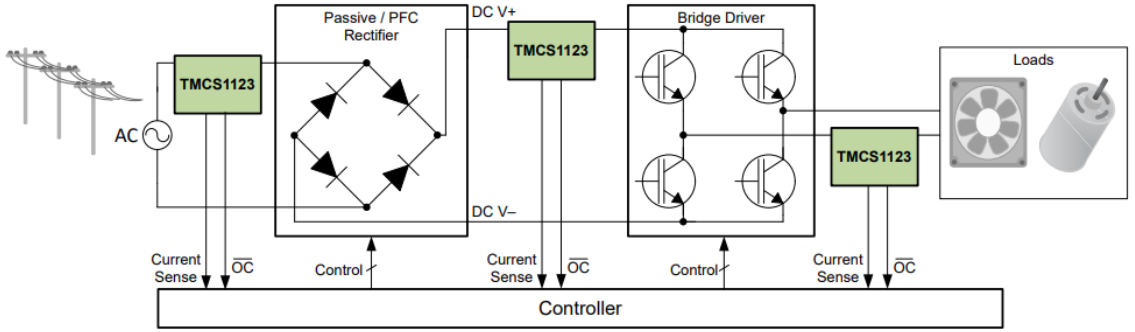


- Second order
- Lossless
- SPWM:
  - Fundamental at 60Hz
  - Harmonics around multiples of 200kHz
- 1mH and 0.7µF → ~6000 Hz cutoff
- ~10% max inductor current ripple
  - Balance inductor size/$ and core losses

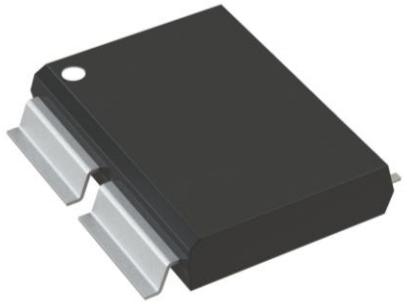


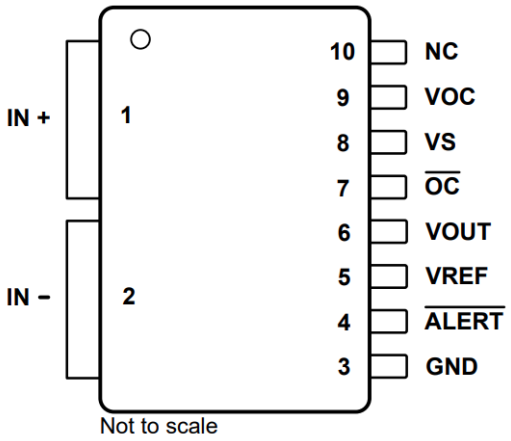
$$f_c = \frac{1}{2\pi\sqrt{LC}}$$

Current Sensing



- Simple current sensing for open-loop monitoring
- **TI TMCS1123:**
  - Hall effect sensor
  - 250kHz signal bandwidth
  - High current:
    - Positive and negative





PRODUCT	SENSITIVITY	ZERO CURRENT OUTPUT VOLTAGE	I_{IN} LINEAR MEASUREMENT RANGE(1)	
			V_S = 5V	V_S = 3.3V
TMCS1123A1A	25mV/A	2.5V	±96A(2)	–96A to 28A(2)
TMCS1123A2A	50mV/A		±48A(2)	–48A to 14A(2)
TMCS1123A3A	75mV/A		±32A	–32A to 9.3A
TMCS1123A4A	100mV/A		±24A	–24A to 7A
TMCS1123A5A	150mV/A		±16A	–16A to 4.7A
TMCS1123B1A	25mV/A	1.65V	–62A to 130A(2)	±62A(2)
TMCS1123B2A	50mV/A		–31A to 65A(2)	±31A
TMCS1123B3A	75mV/A		–20.7A to 43.3A(2)	±20.7A
TMCS1123B4A	100mV/A		–15.5A to 32.5A	±15.5A
TMCS1123B5A	150mV/A		–10.3A to 21.7A	±10.3A
TMCS1123C1A	25mV/A	0.33V	–9.2A to 183A(2)	–9.2A to 115A(2)
TMCS1123C2A	50mV/A		–4.6A to 91.4A(2)	–4.6A to 57.4A(2)
TMCS1123C3A	75mV/A		–3.1A to 60.9A(2)	–3.1A to 38.3A(2)
TMCS1123C4A	100mV/A		–2.3A to 45.7A(2)	–2.3A to 28.7A
TMCS1123C5A	150mV/A		–1.5A to 30.5A	–1.5A to 19.1A

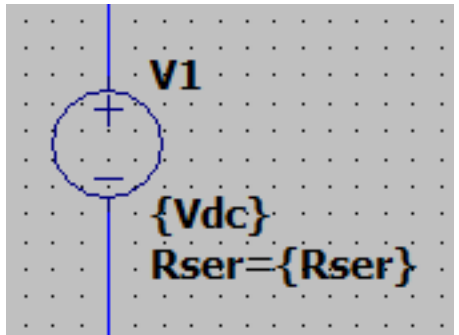
Maximize sensitivity (maximize ADC resolution utilization) while measuring up to $I_{ds,max}$

4/9

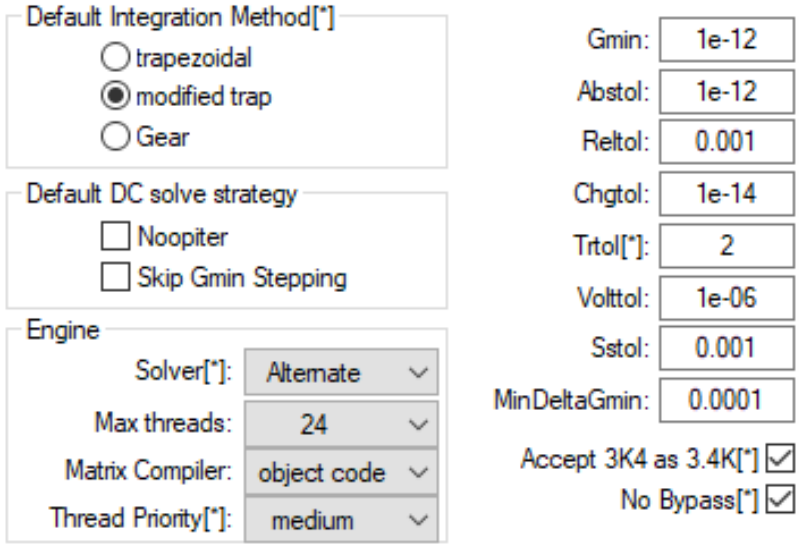
Simulations

Convergence

- Challenge: Slow simulation speed!
  - Complex gate driver and GaN models
- Solution:
  - Trade-off accuracy for time
  - Try different solvers
  - Analyze over a single cycle
  - Add series resistors to voltage sources → modelled as current sources

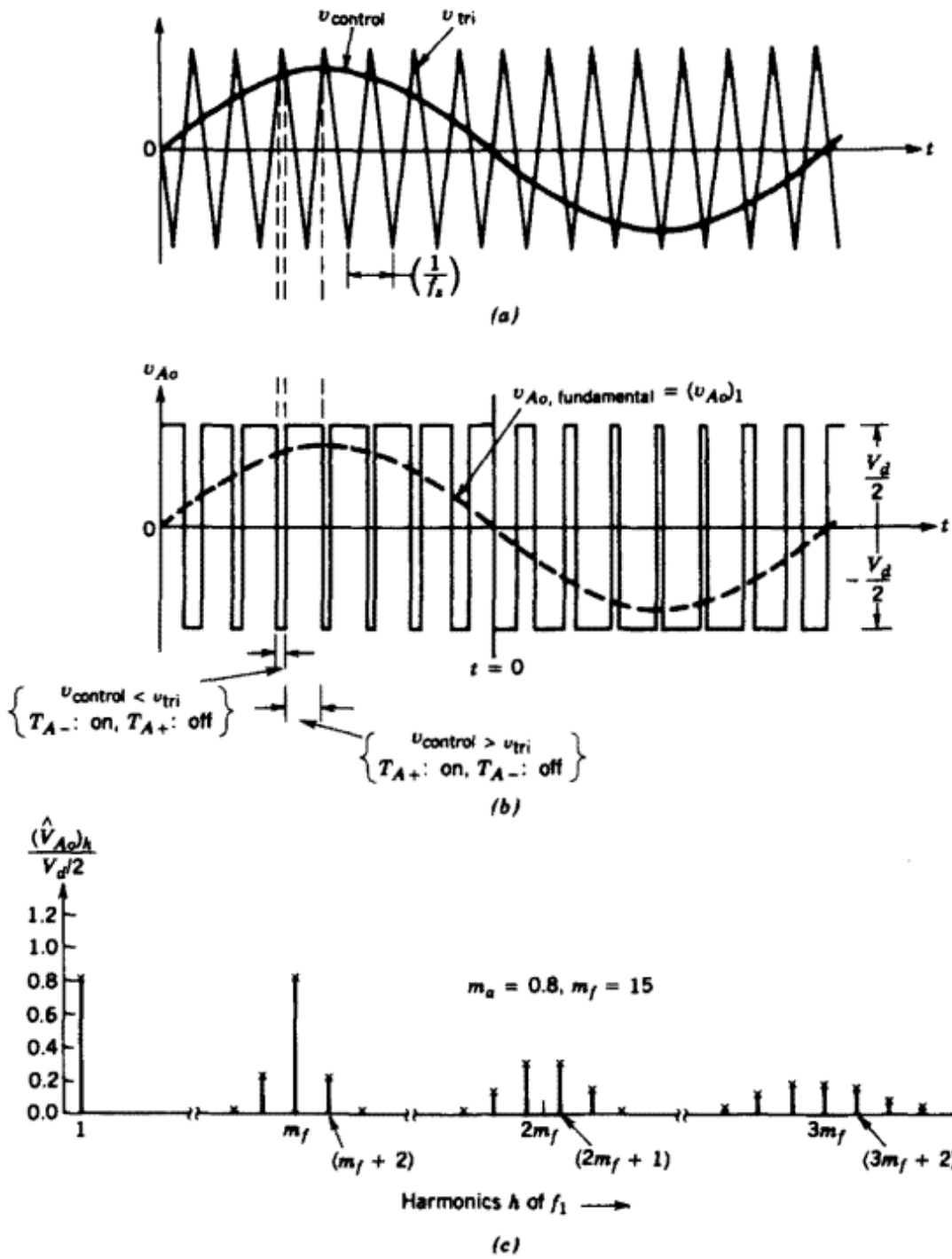


Simulation Speed: 6.27211 ps/s



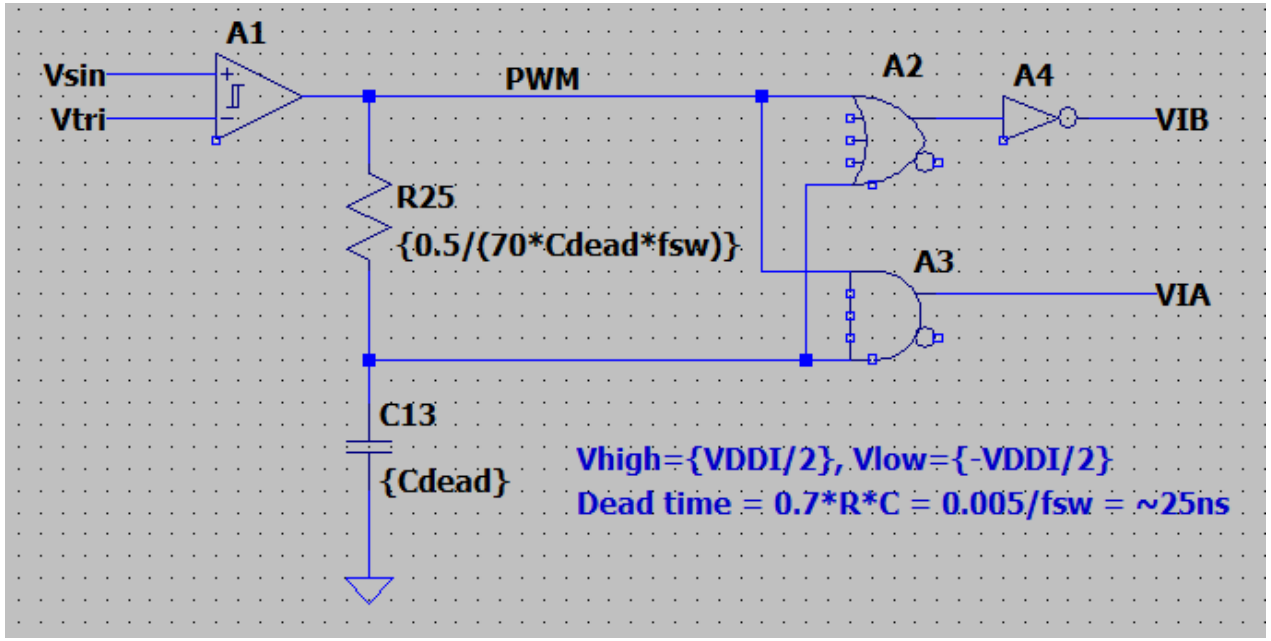
SPWM

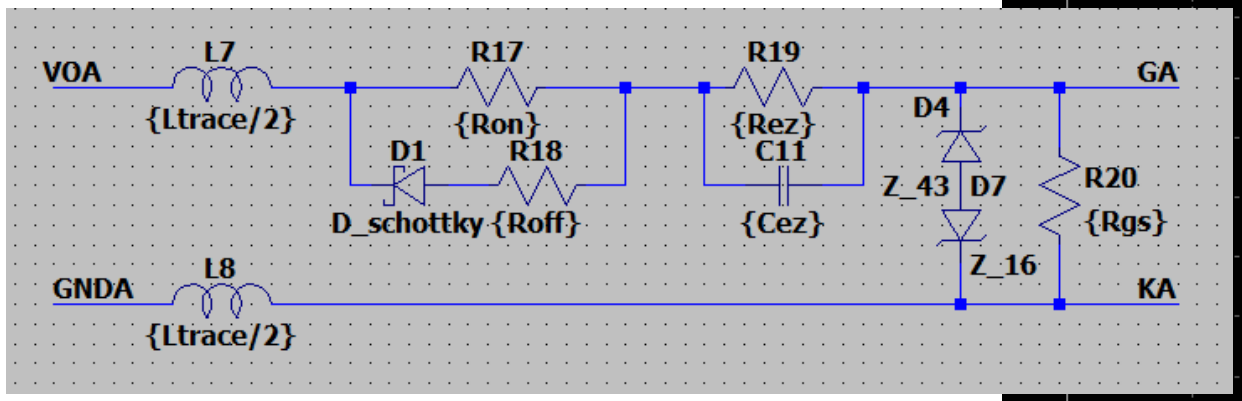
- f_1 = 60 Hz
- $f_{sw} \approx$ 200 kHz
- $m_f = f_{sw}/f_1 = 3333$
  - Avoid non-integer value (especially for AC motors) → no subharmonics of f_1
  - Odd integer: odd and half-wave symmetries → no even harmonics
- $m_a = V_{ref}/V_{tri} = 0.95$
  - Avoid overmodulation (>1.0), o/w difficult to filter harmonics

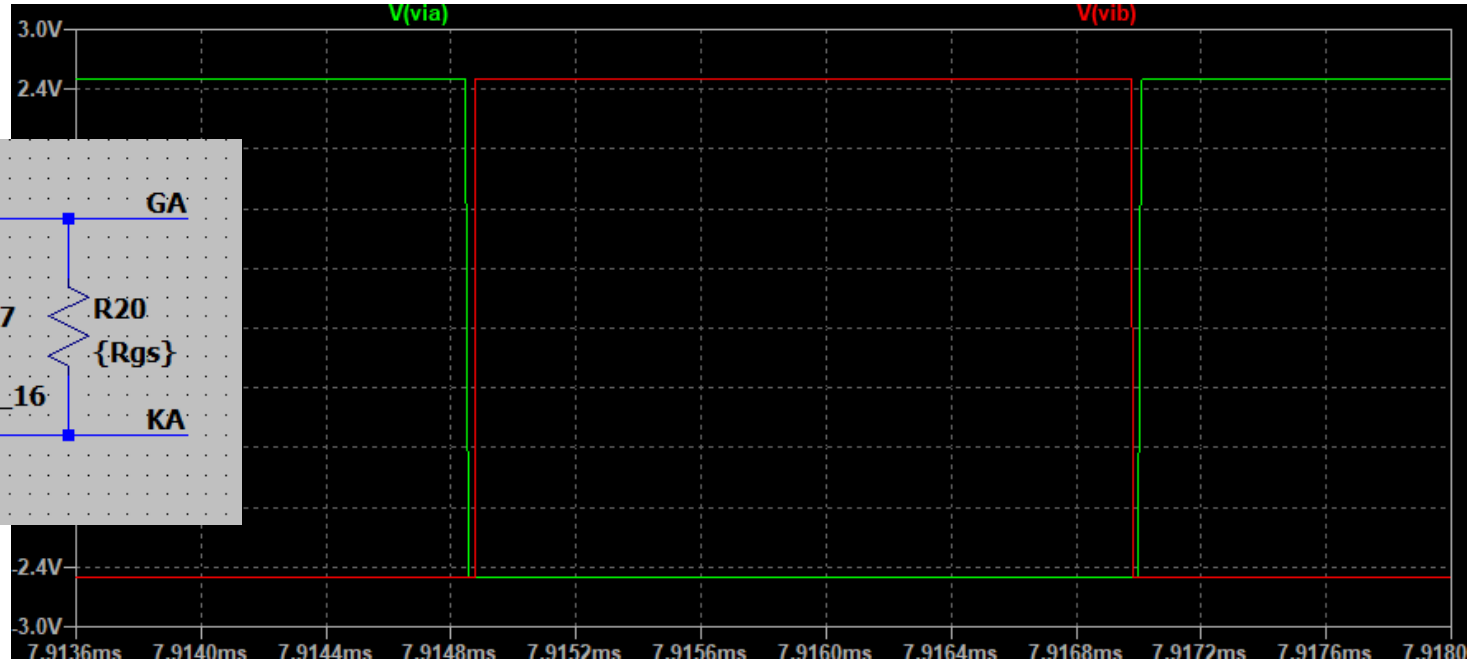


Gate Driving

- Ideal PWM input with DT
- → Gate driver model
- → Level-shifting circuit
- Make use of variables

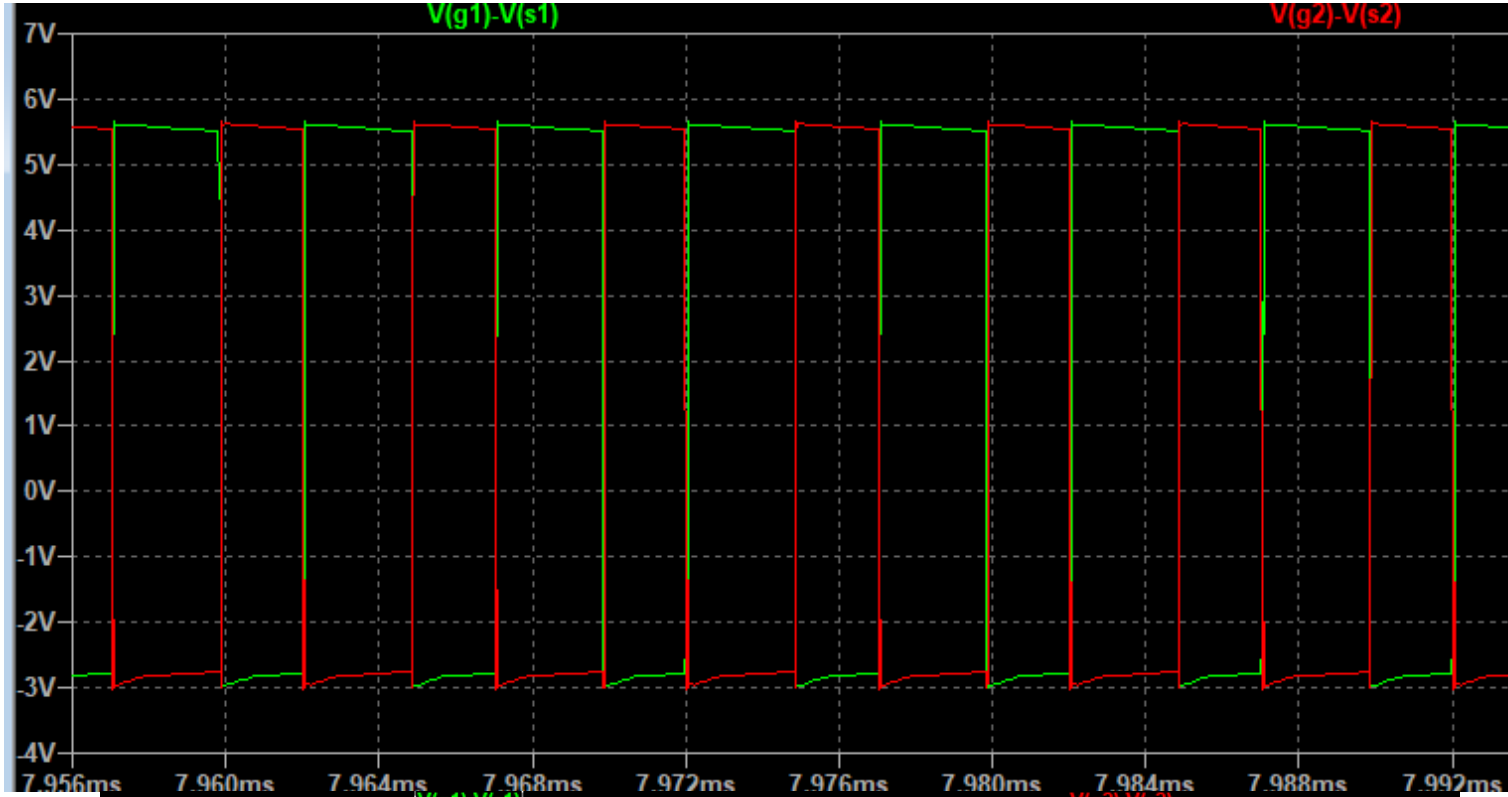


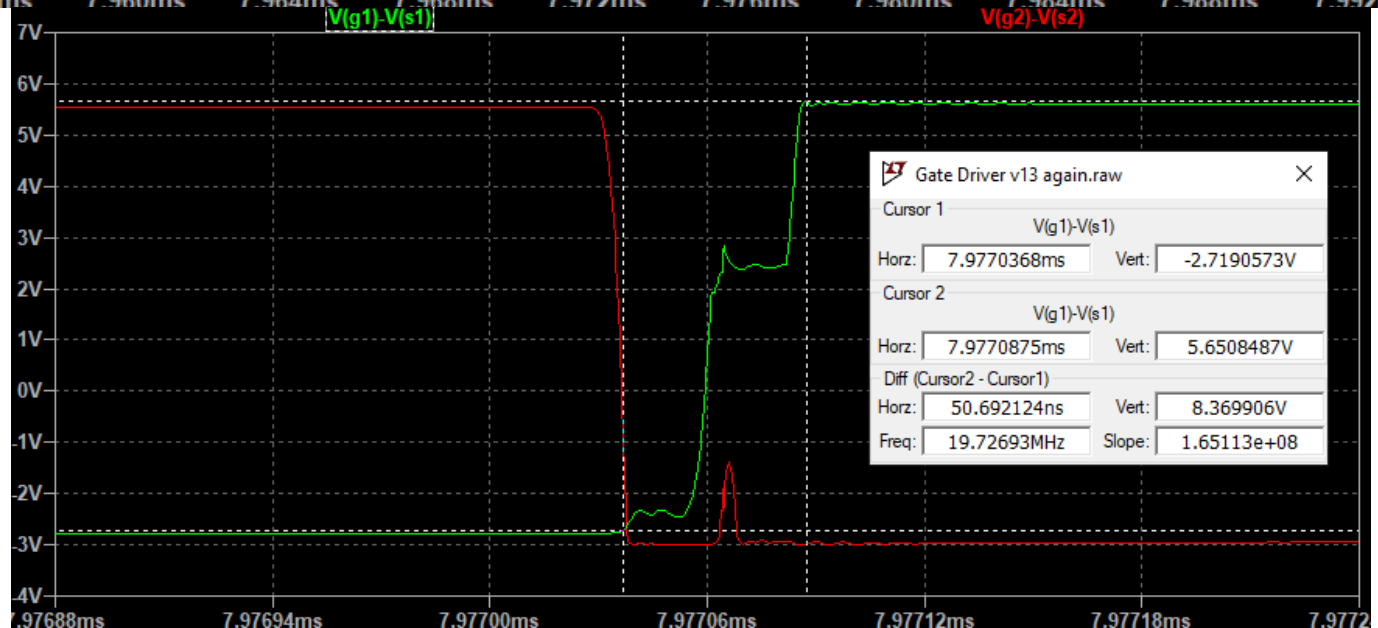




Gating Dynamics

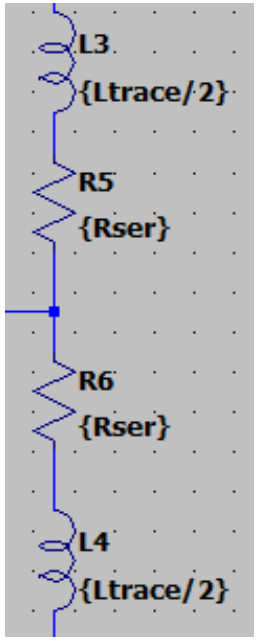
- Level-shifting:
  - As desired
- Gate resistances:
  - Underdamping
- Miller plateau:
  - As desired
- Ground bounce:
  - Minimal
  - Below V_{th}

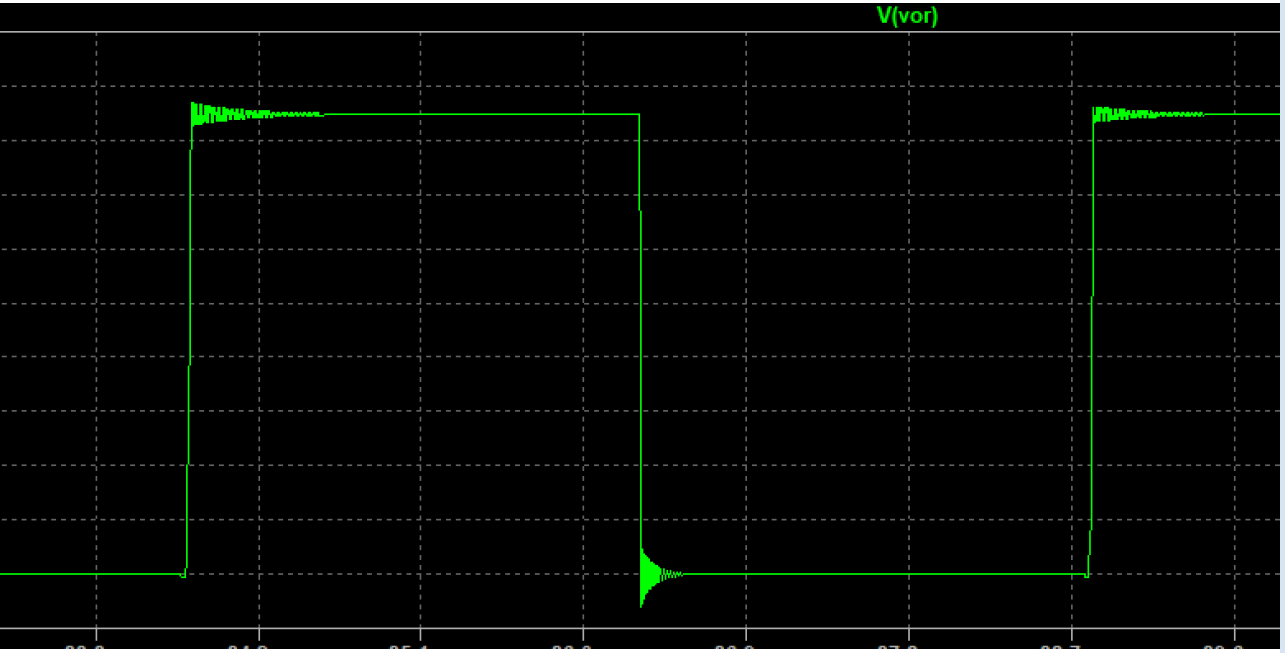


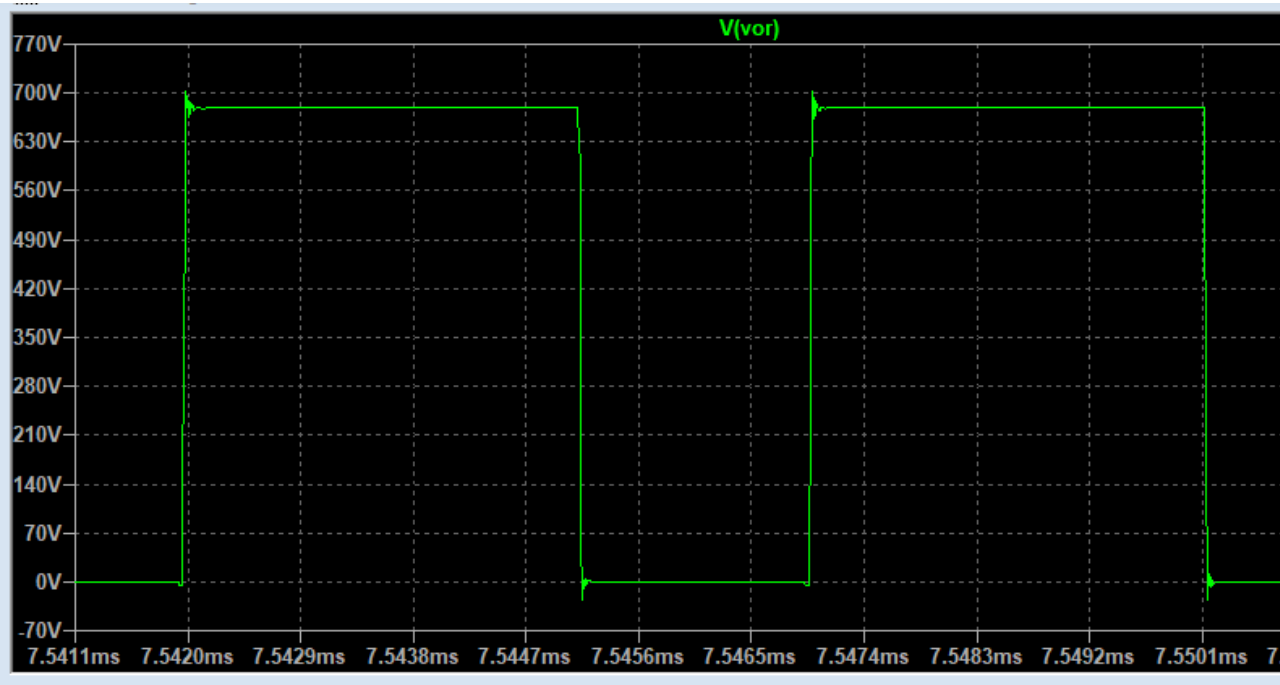


Switching Node

- Modelled trace inductances
  - Iterative process with PCB layout
  - Worst case ~10 nH
- Damped ringing with snubbers

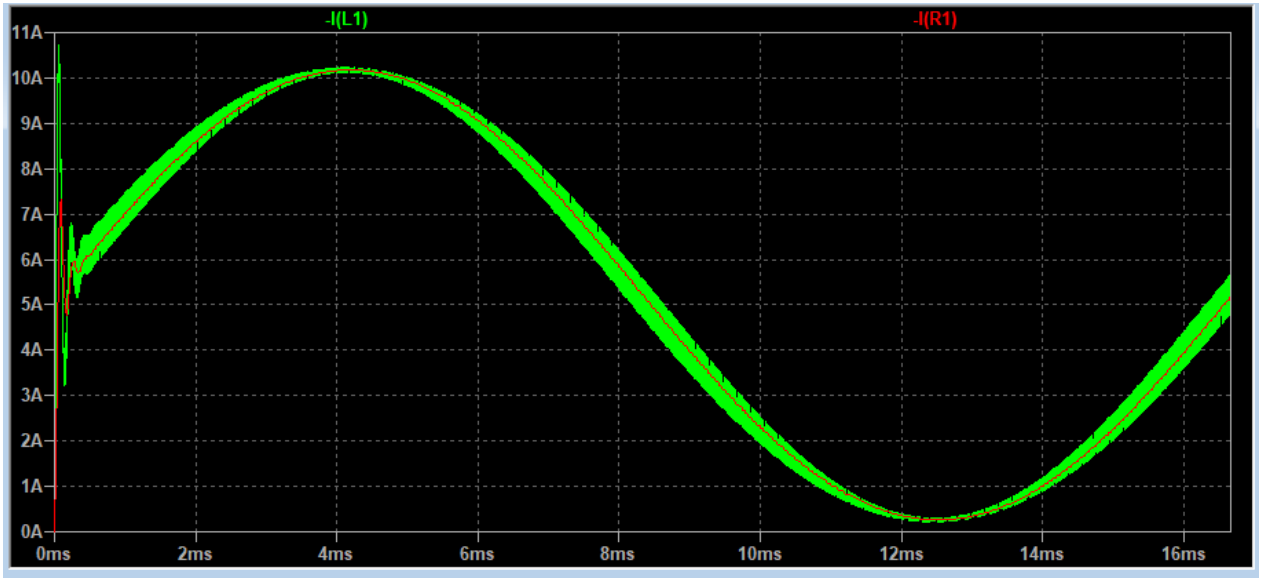


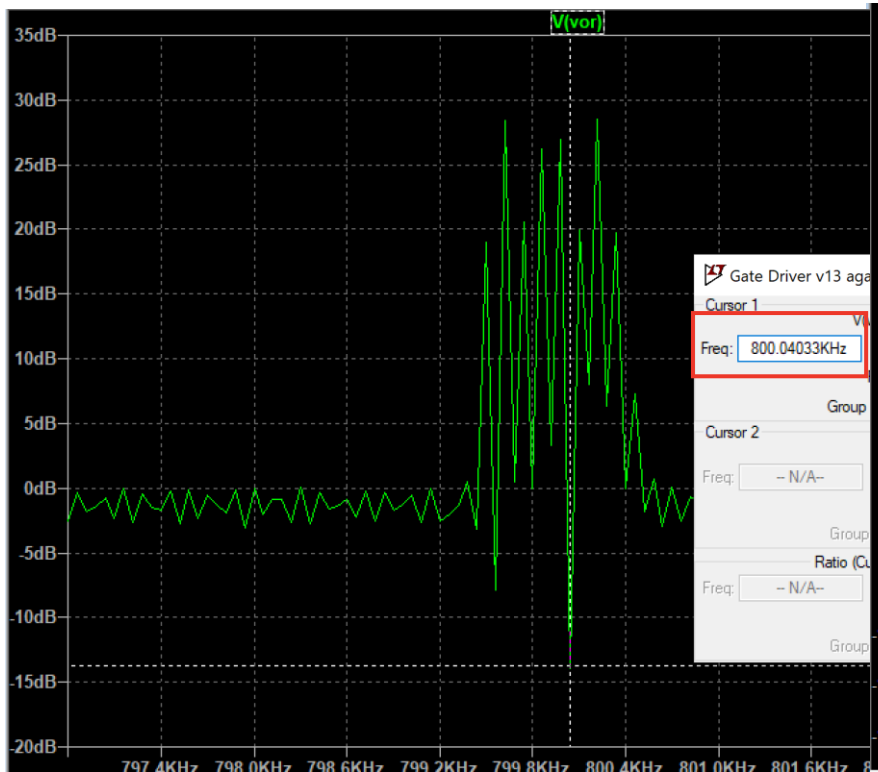


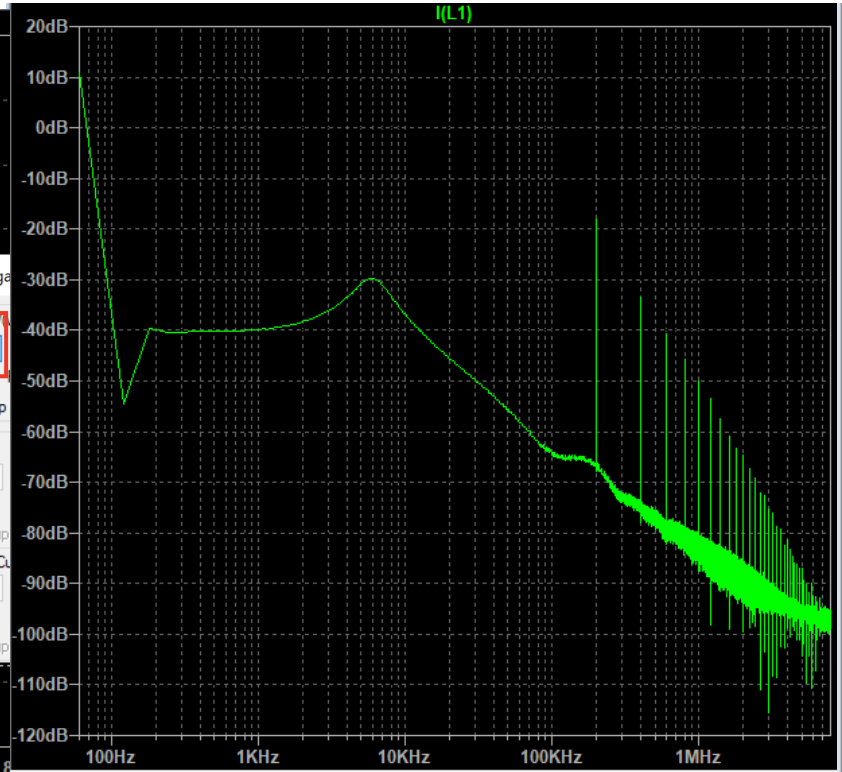


Harmonics Analysis

- Clean inductor current ripple
- FFT shows proper filtering
  - Even harmonics suppressed too

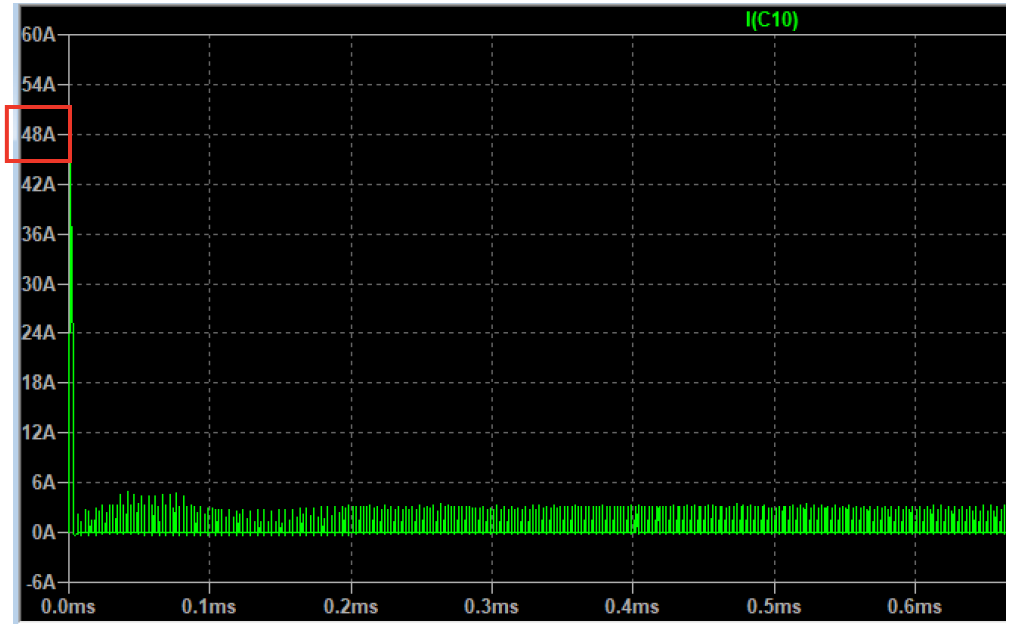


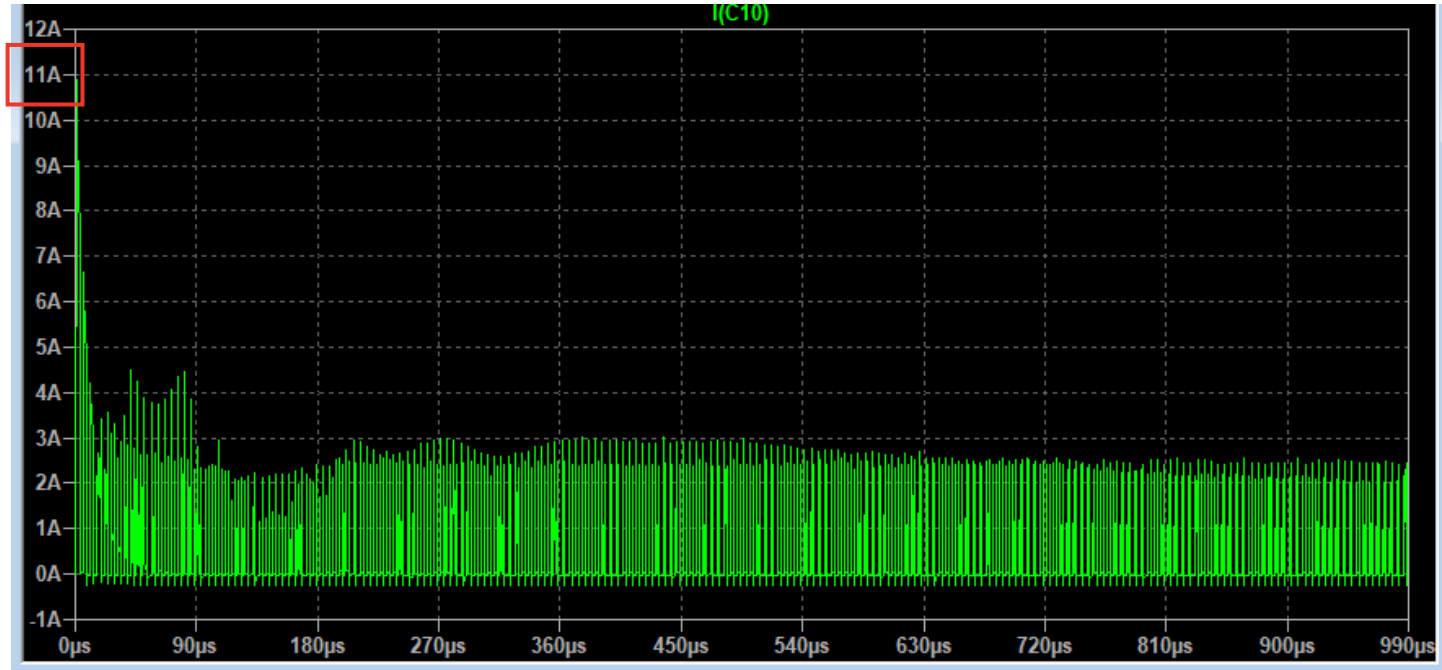




Current Analysis

- I_{CB} initial spike limited by R_B
- Extract average and peak currents for PCB trace width design
- Extract resistor powers for sizing



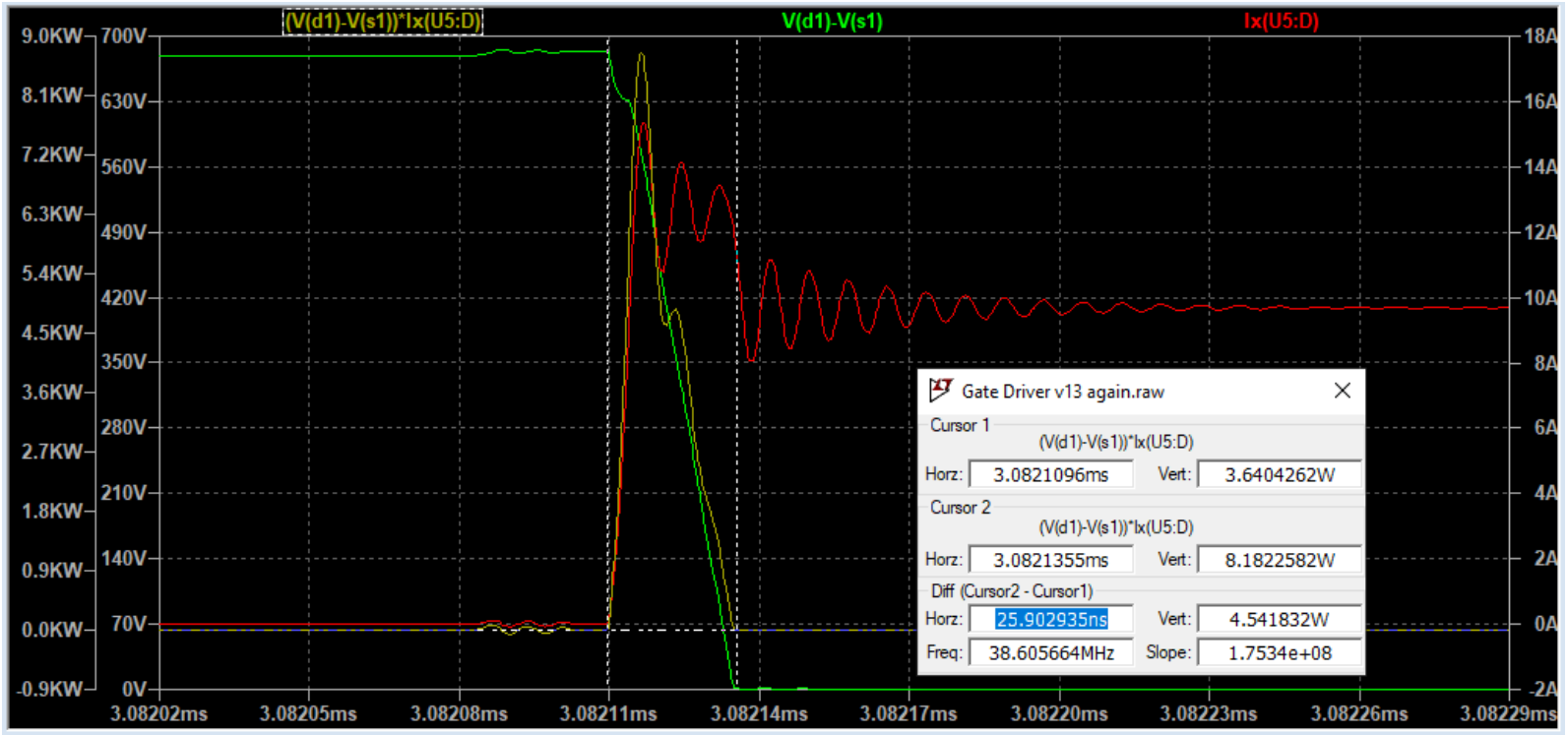


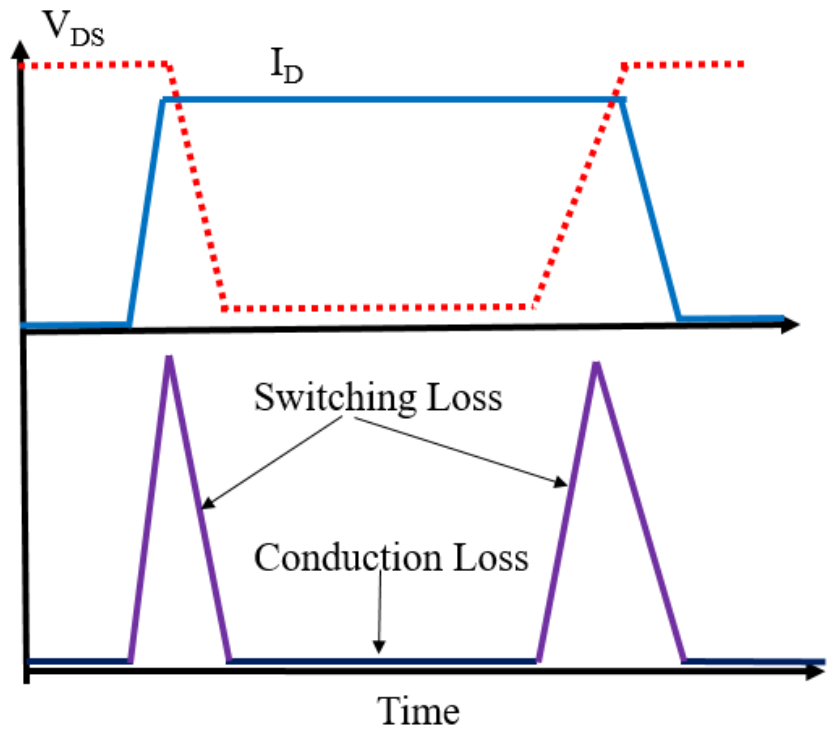
Power Analysis

- Efficiency = 99.2%
- >10W per switch
  - Mostly P_{sw} ($R_{ds,on}$ = 120 mΩ)

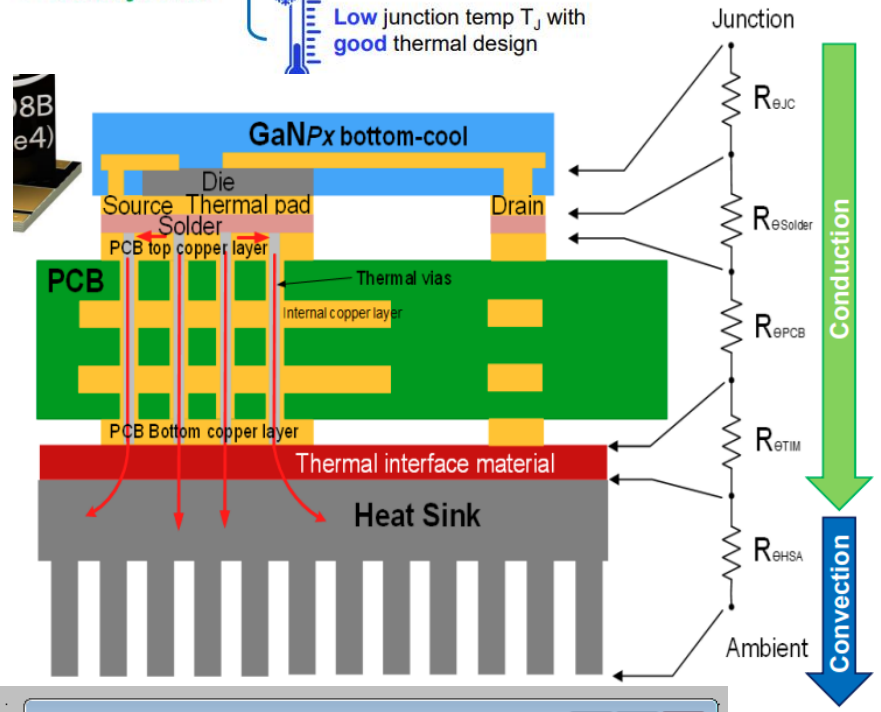
$$P_{\mathrm{INV(cond)}} = I_{\mathrm{rms}_f}^2 R_{DS} + \sum_{n=1}^{3} I_{\mathrm{rms}(n)}^2 R_{DS}.$$

$$P_{\mathrm{INV}(sw)} = V_{dc} I_{\mathrm{rms}} \frac{(t_{\mathrm{rise}} + t_{\mathrm{fall}})}{2} f_{sw}$$

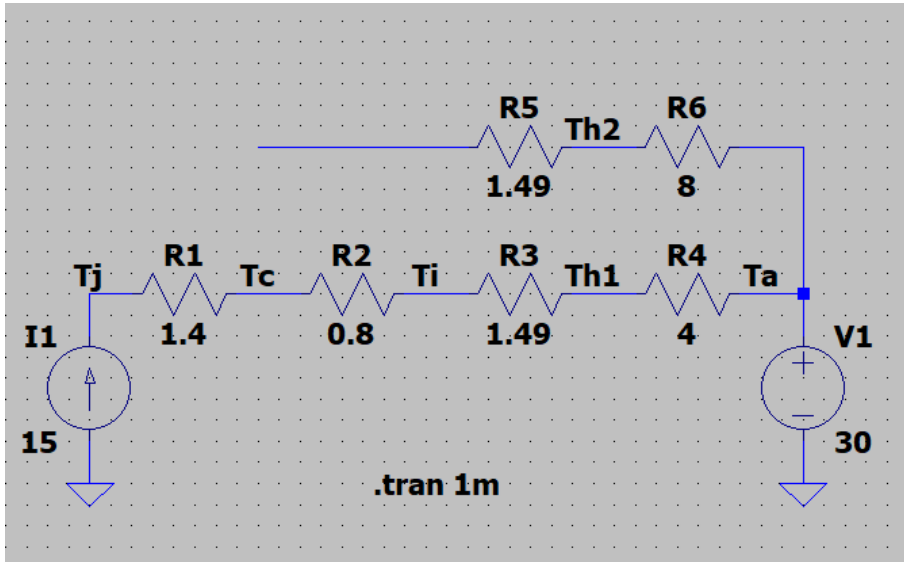


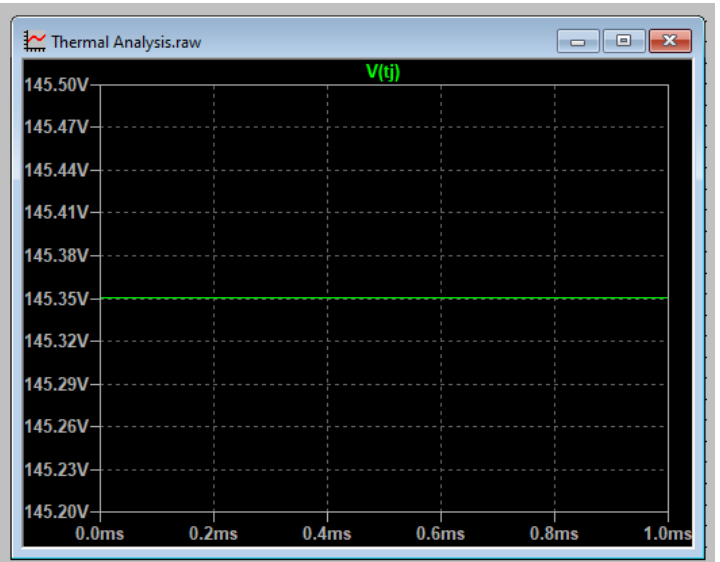


Thermal Analysis

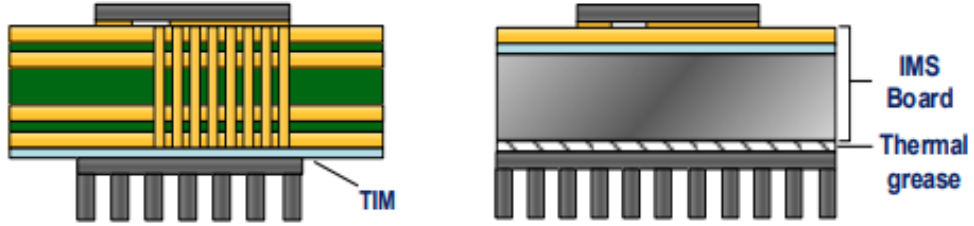


- No thermal model provided ☹
- Iterative process with PCB layout
  - Thermal vias, heatsink and TIM selection
- Design for 15W, T_A = 30°C as a FOS
- T_{jmax} = 150 °C



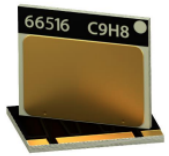


Heatsink and TIM Selection

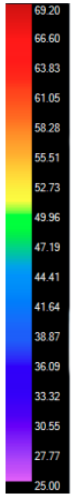


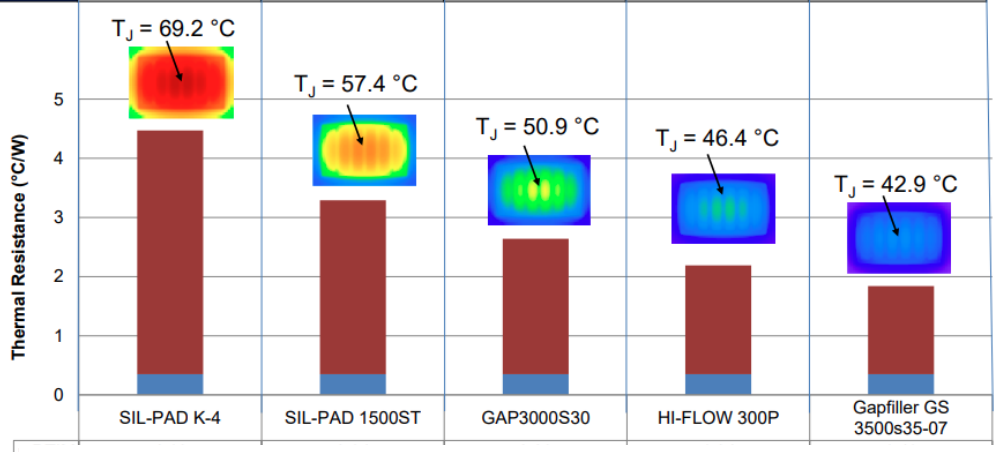
- Metal-based PCB?
  - ↓↓ $R_{\theta JHS}$ but ↑↑$
- **Hi-Flow THF 1600P:**
  - Thermally conductive, electrically isolated
  - 0.102 mm thickness
  - 1.6 W/m·K
  - Non-liquid
- Heatsink:
  - Black (for thermal camera)
  - PCB layout ⇄ HS size

- GS66516T is applied with 10 W power loss on it
- T_{HS} = 25 °C

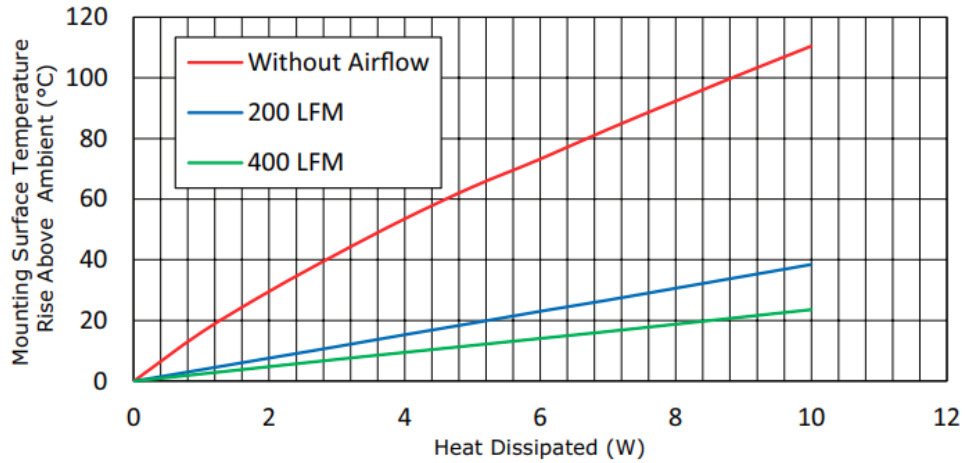


	SIL-PAD K-4	SIL-PAD 1500ST	GAP3000S30	HI-FLOW 300P	GAPFILLER GS 3500S35-07
TIM Thickness (mm)	0.152	0.203	0.25	0.102	0.178
Thermal conductivity (W/m·K)	0.9	1.8	3.0	1.6	3.6





Key parameters for TIM material selection: dielectric strength, mechanical strength, and cost.



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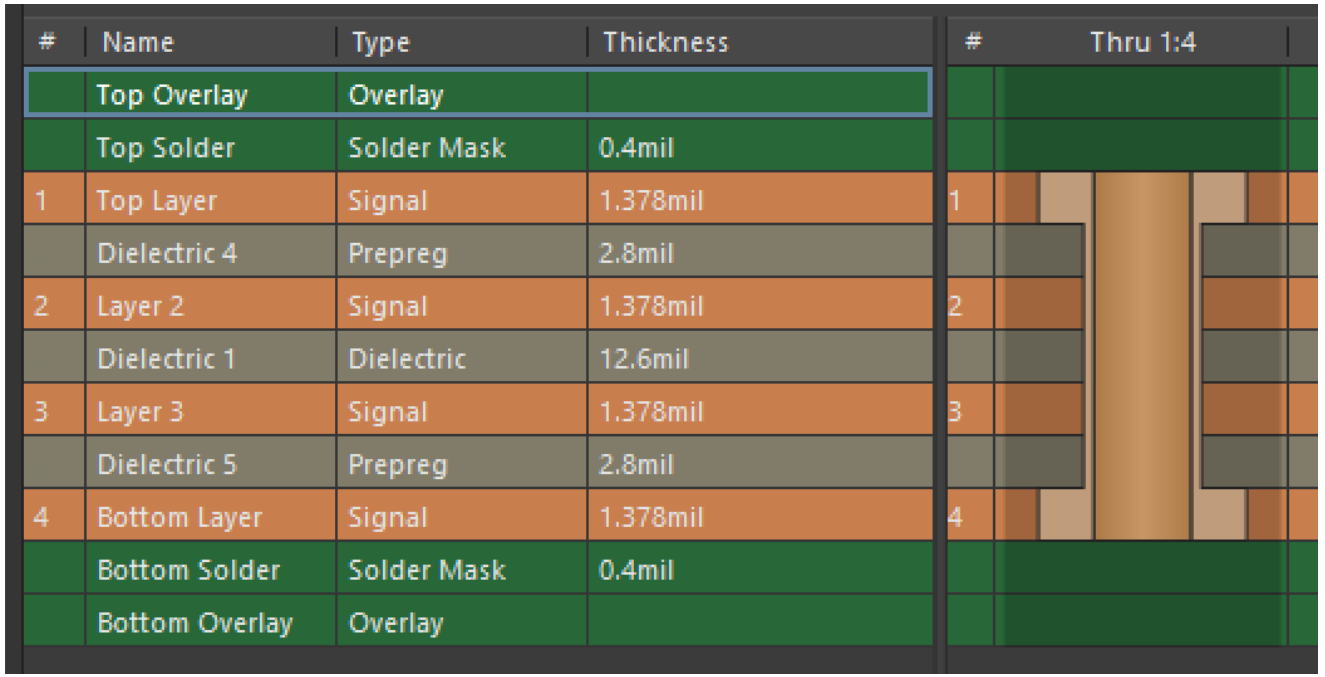
PCB Design

Layer Stack

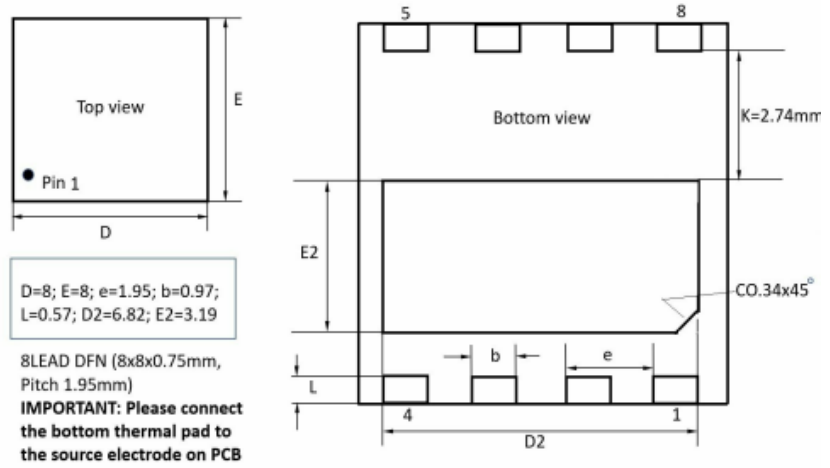
- Operating frequency in the kHz → don't worry about impedance and length matching
- 4 layers:
  - Top
  - PWR
  - GND
  - Bottom
- Benefits:
  - Simplify routing
  - Increase density
  - Acceptable cost

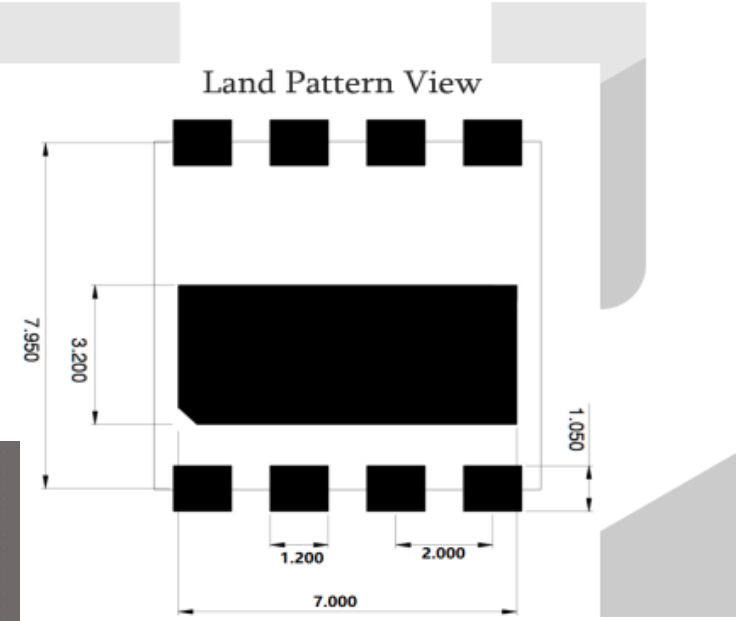


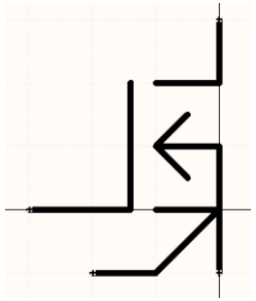
#	Name	Type	Thickness
	Top Overlay	Overlay	
	Top Solder	Solder Mask	0.4mil
1	Top Layer	Signal	1.378mil
	Dielectric 4	Prepreg	2.8mil
2	Layer 2	Signal	1.378mil
	Dielectric 1	Dielectric	12.6mil
3	Layer 3	Signal	1.378mil
	Dielectric 5	Prepreg	2.8mil
4	Bottom Layer	Signal	1.378mil
	Bottom Solder	Solder Mask	0.4mil
	Bottom Overlay	Overlay	

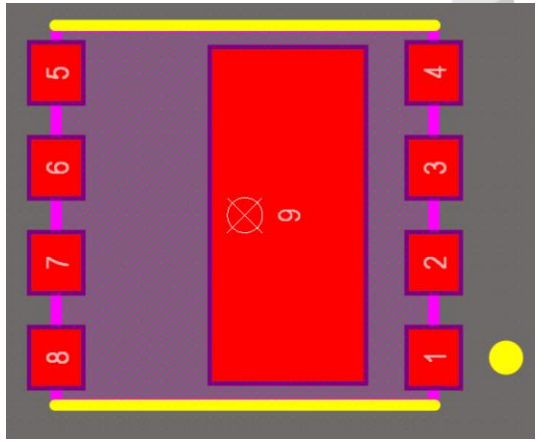
Components

- Created schematic and footprint libraries:
  - Consistency
  - Gate driver: *IPC compliant footprint wizard*
  - GaN DFN: manual footprint creation
  - Use datasheets for dimensions
- BOM: given approved supplier list
  - Quality control
  - Leverage partnerships



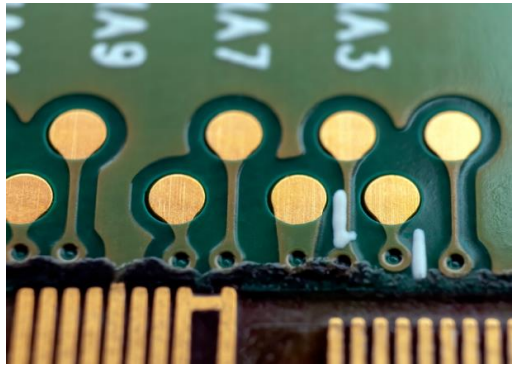


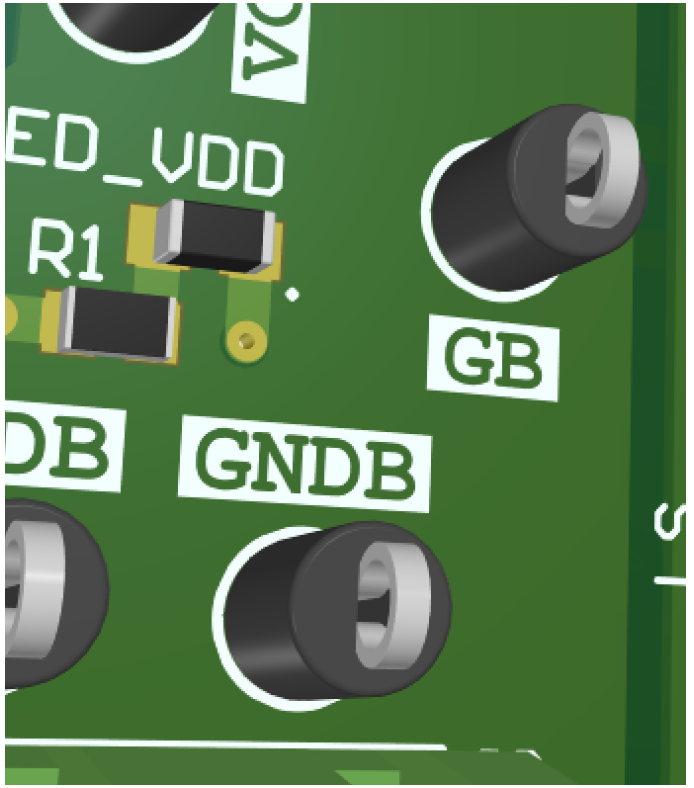




Testing Points

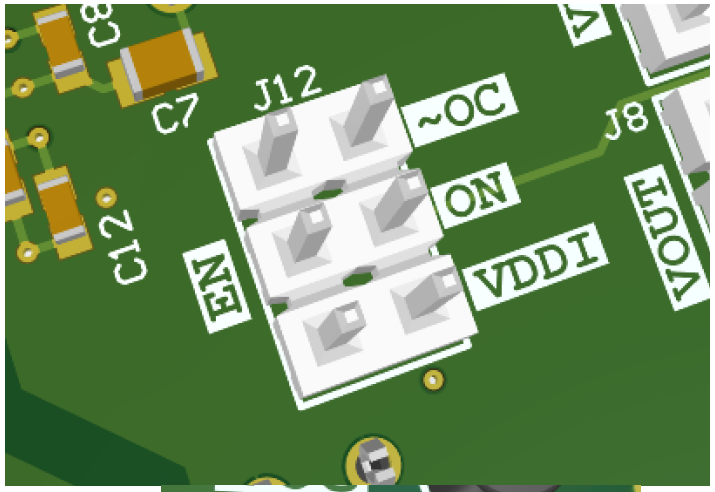
- Design for testing (DFT) aligns with project objective
- GaN gate probing: minimize probe loop
- Test points for:
  - Gate driver pins
  - Gate pins
  - Hall sensor pins
  - Power and grounds
- Considered test pads:
  - Difficult to probe

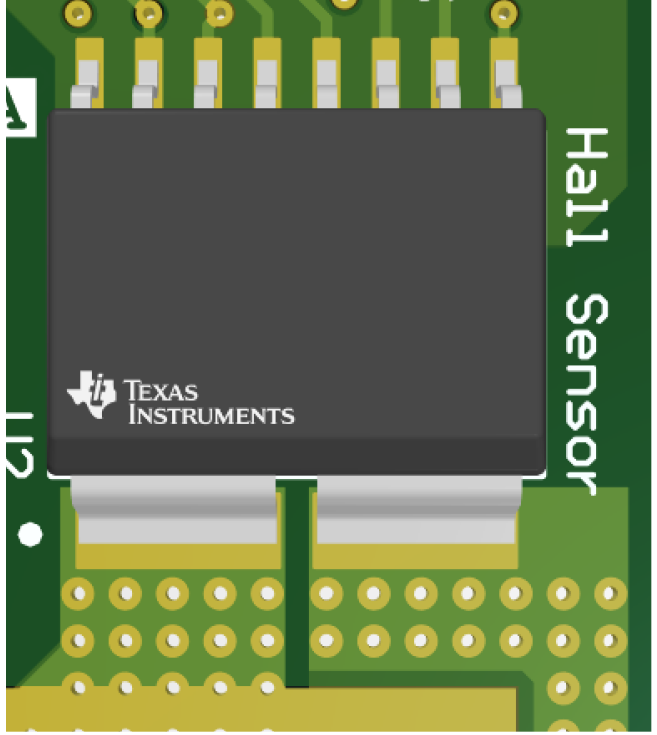


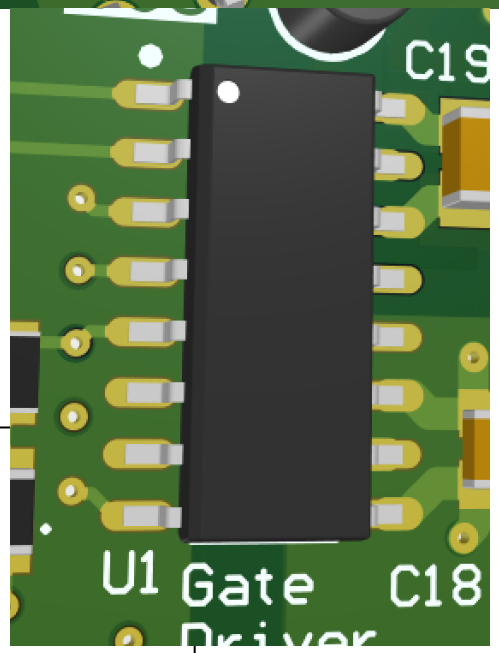


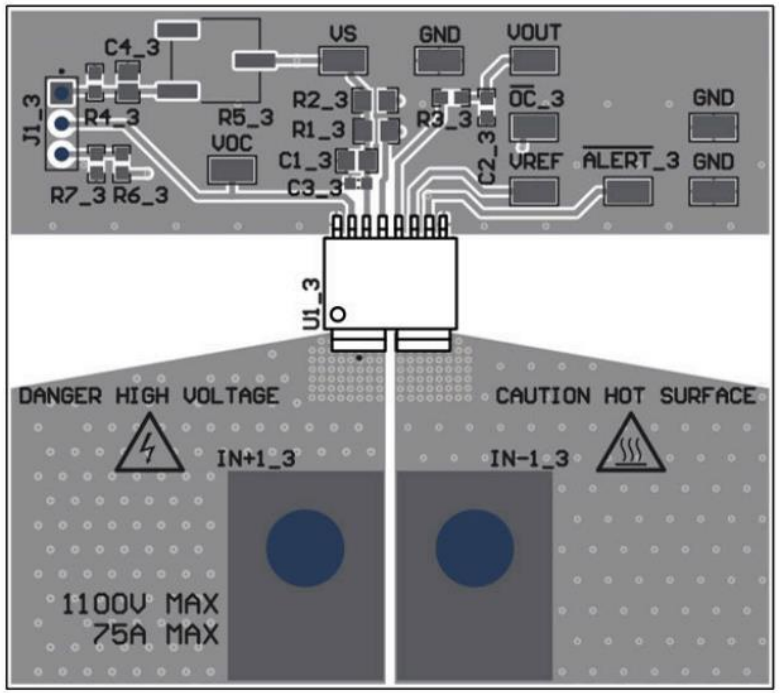
ICs

- Datasheets for layout and PSU guidelines
- Gate driver DFT
  - Header for EN signal
- Hall sensor
  - 0.5% precision resistor divider to set V_{OC}







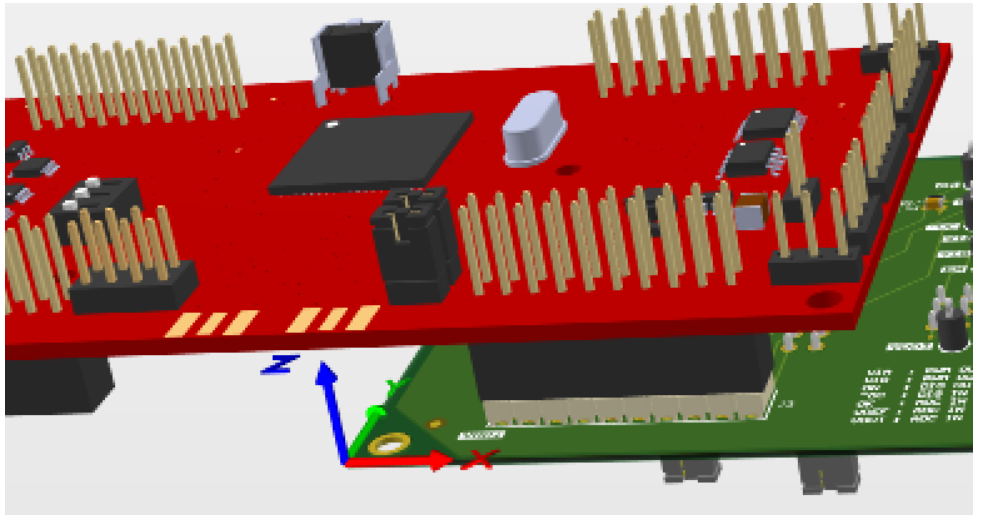


$$V_{OC} = \frac{S \times I_{OC}}{2.5}$$

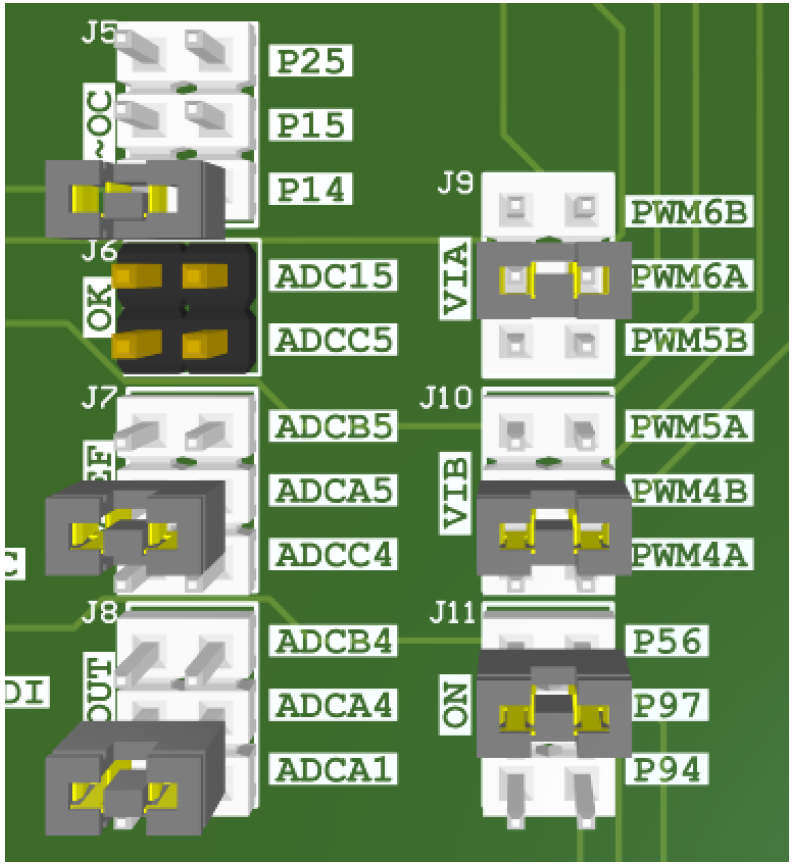
where

- S is the device sensitivity in mV/A.
- I_{OC} is the desired overcurrent threshold.
- V_{OC} is the voltage applied that sets the overcurrent threshold.

DSP Connection

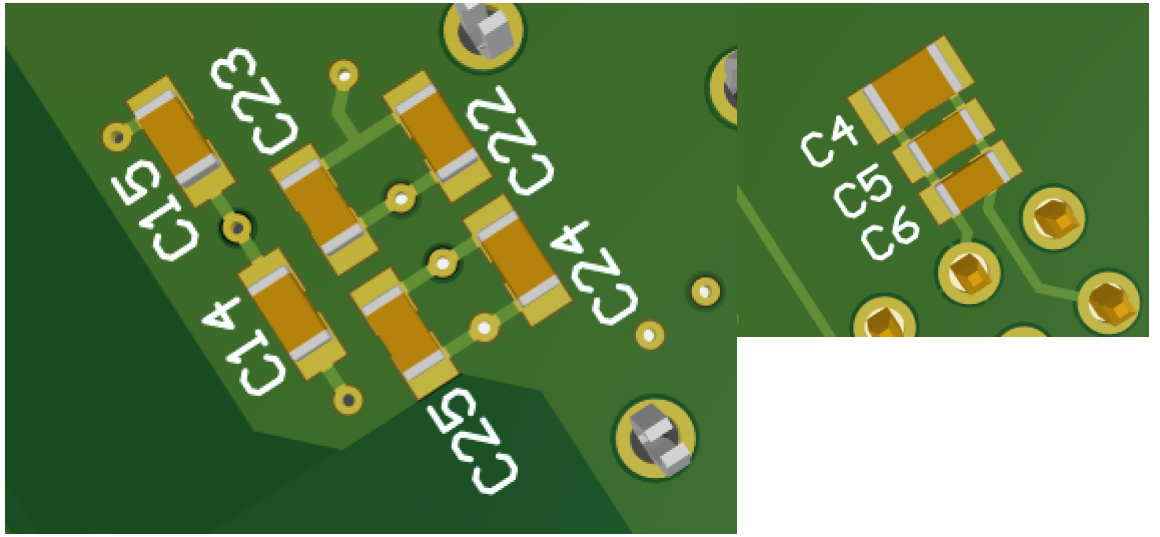


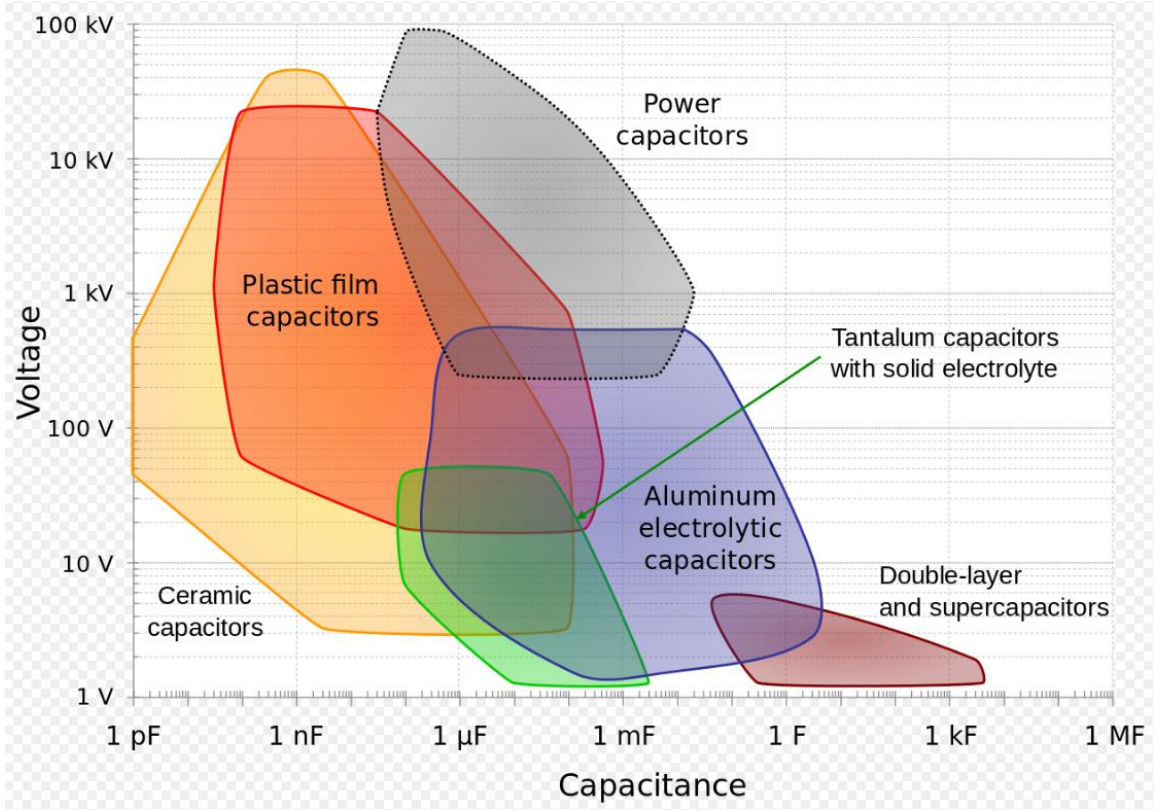
- Options:
  - Jumper wires to headers:
    - Pros: simpler, ↓ board area, ↓ connection count
    - Cons: ↓ noise immunity, ↑ mis/disconnection risk
  - Ribbon cable:
    - Mitigate misconnection risk
  - Daughter board:
    - Mitigate misconnection and noise immunity risks
- Connect half of DSP → future extensions
- Jumpers to change pins in case they fail
  - Part of DFT



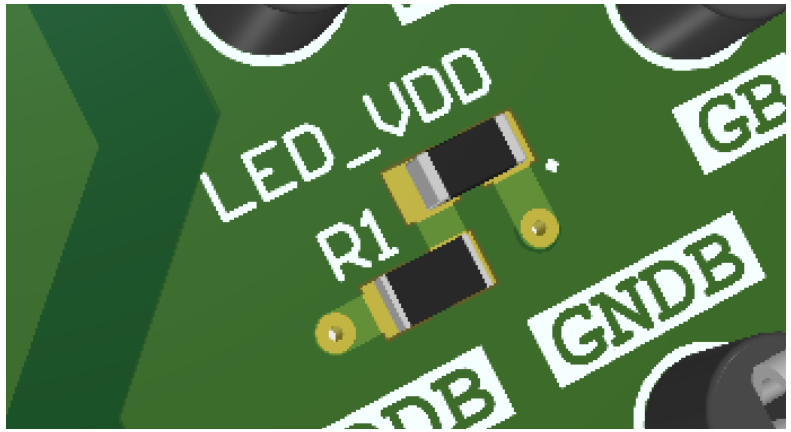
Decoupling Capacitors

- Minimize line *L* and series *R*:
  - Place near DC source pins
  - Place near DC destination pins
- Multiple in parallel → ↓ Total ESR
- Ceramic:
  - ↓ Size
  - ↓ ESR
  - ↑ Reliability
  - ↑ Q at ↑ frequency
- Rated voltage > $2V_c$

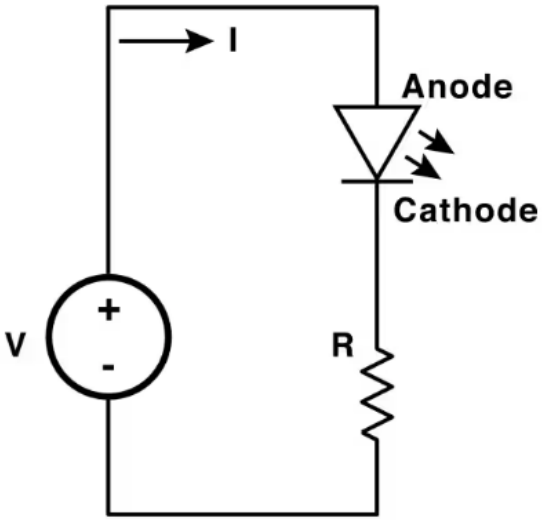




LED Indicators



- For DFT and better user experience
- DSP 3.3V Power
- Driver 12V Power
- Driver 3.3V Enable
- Current-limiting resistors to ensure nominal I_f

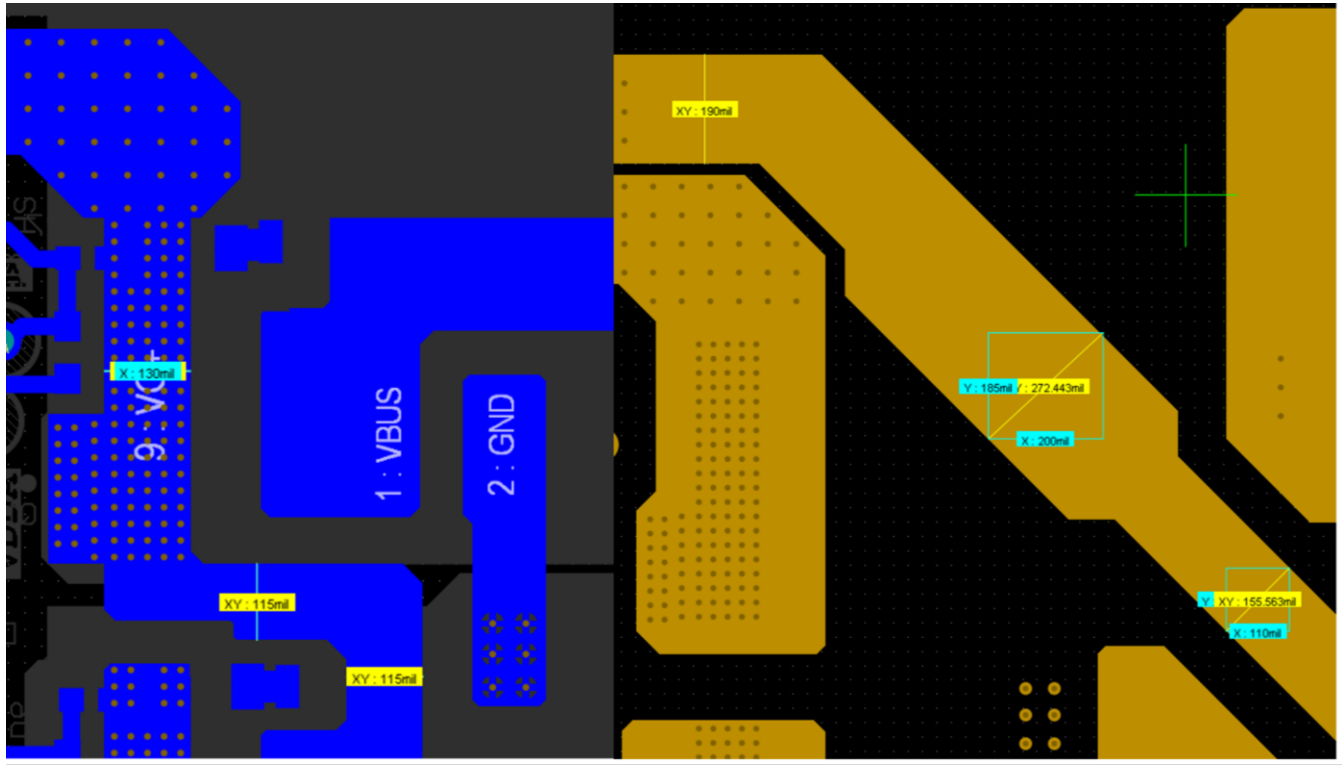


$$R = \frac{V_s - V_f}{I_f}$$

Trace Width

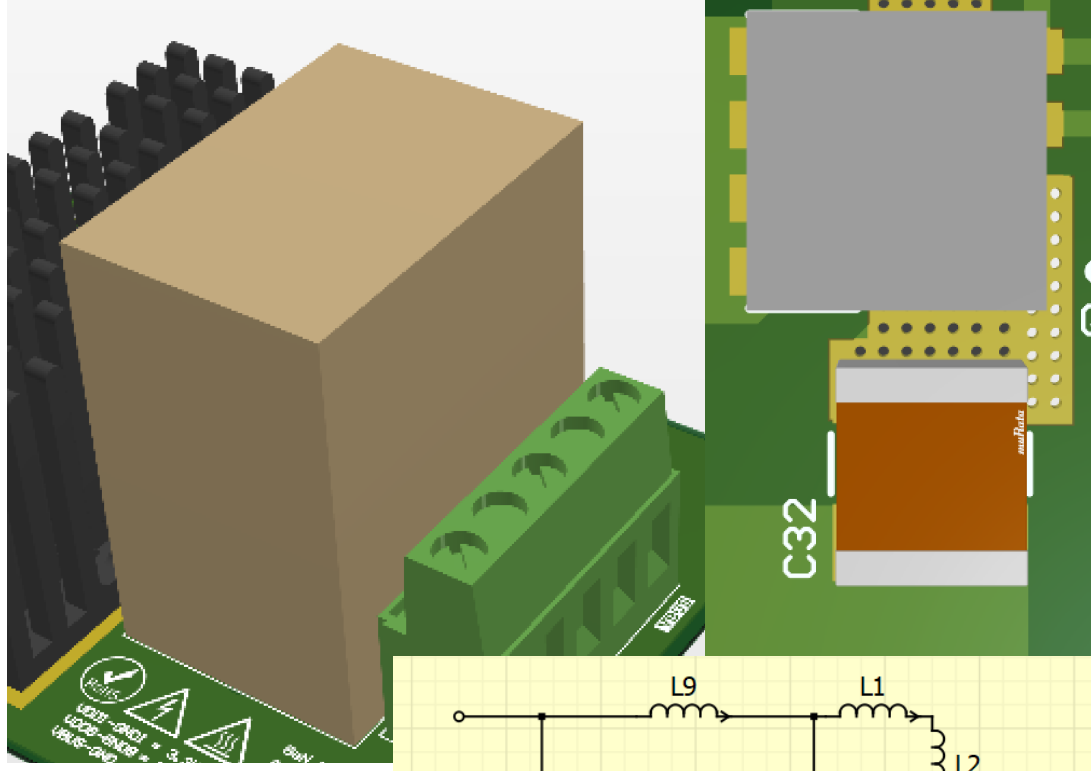
ANSI PCB TRACE WIDTH CALCULATOR							
Input Data			Results Data				
				Internal Traces		External Traces	
Field	Value	Units	Trace Data	Value	Units	Value	Units
Current (max. 35A)	5	Amps	Required Trace Width	290.44	mil	111.65	mil
Temperature Rise (max. 100°C)	10	°C	Cross-section Area	390.29	mil²	150.03	mil²
Cu thickness	1	oz/ft²	Resistance	0	Ω Ohms	0	Ω Ohms

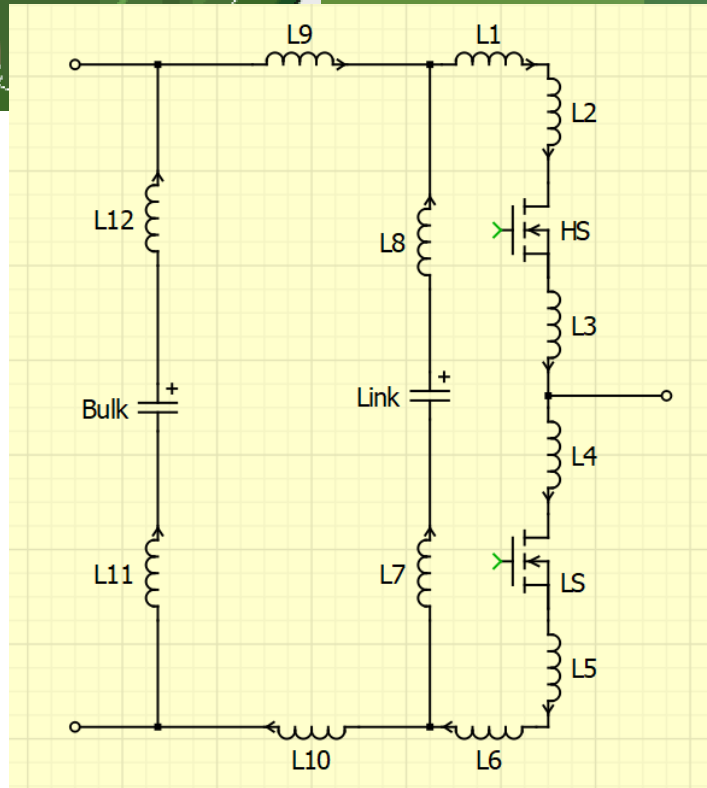
- IPC-2221 standard
- Power traces: design for 10°C rise @5A as a FOS
- Current shared across layers
  - Sum widths for effective
- Driver output current:
  - <50 mA average (sim)
  - <1.6 A peak (sim)
  - Design for peak → 28 mil



DC Bus Capacitors

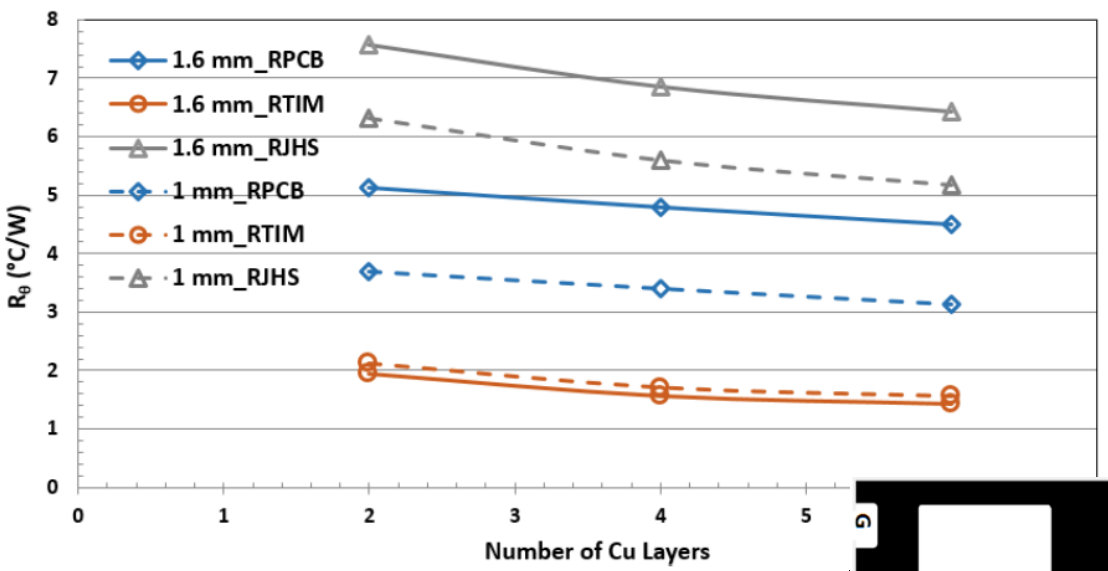
- Minimize power loop inductance:
  - Commutate current as fast as possible
  - Avoid switch overvoltage during DT
- Bulk (film) and links (ceramic)
  - Film: ↑ *dv/dt*, ↑ current, ↓ self-inductance
- Polygons:
  - Maximize V_{bus} to GND overlap
  - Minimize V_{bus} or GND overlap with switch node!

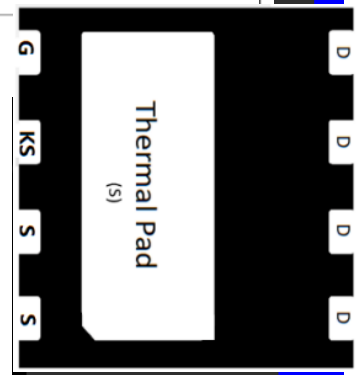


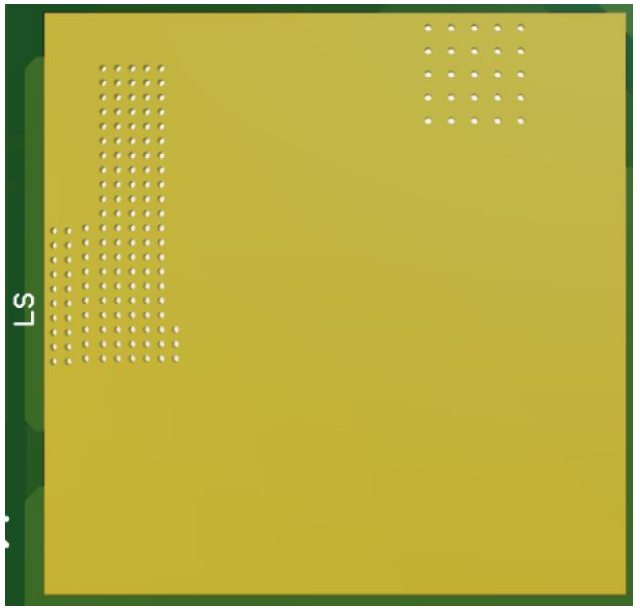


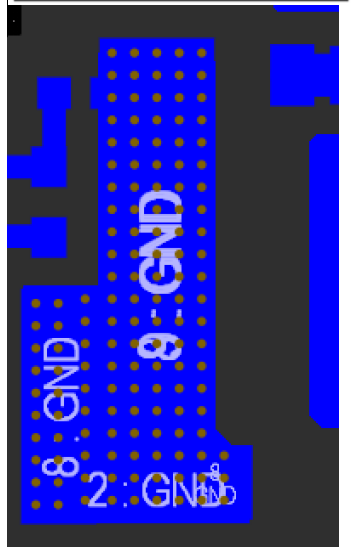
Thermal Vias

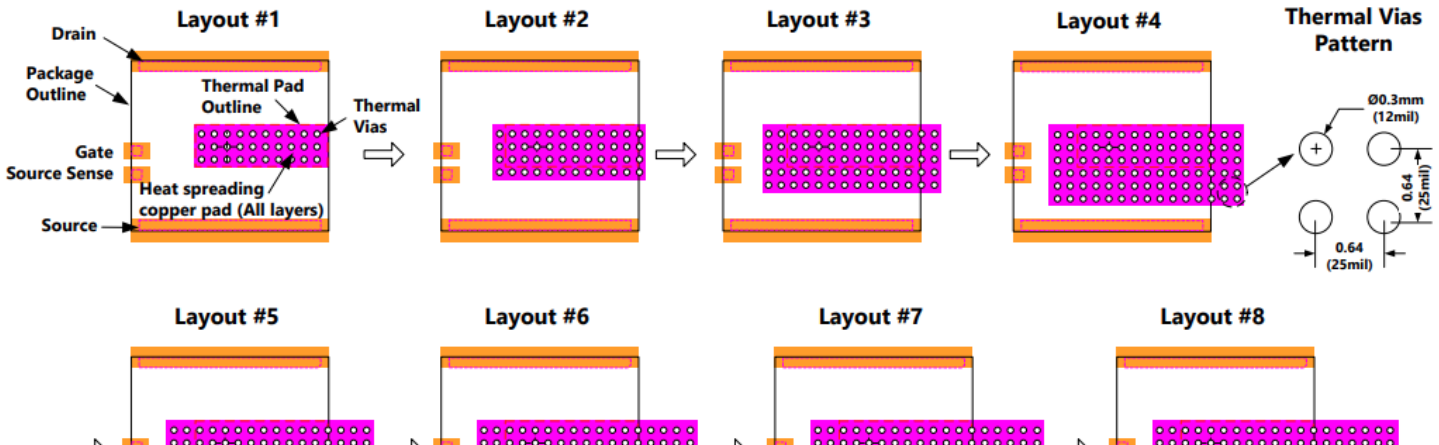
- Bottom-cooled devices
  - → thermal vias → heatsink pad
- Maintain distance from drain pin
- Internal copper layers
  - ↑ Vertical heat transfer
  - ↑ Horizontal heat spreading



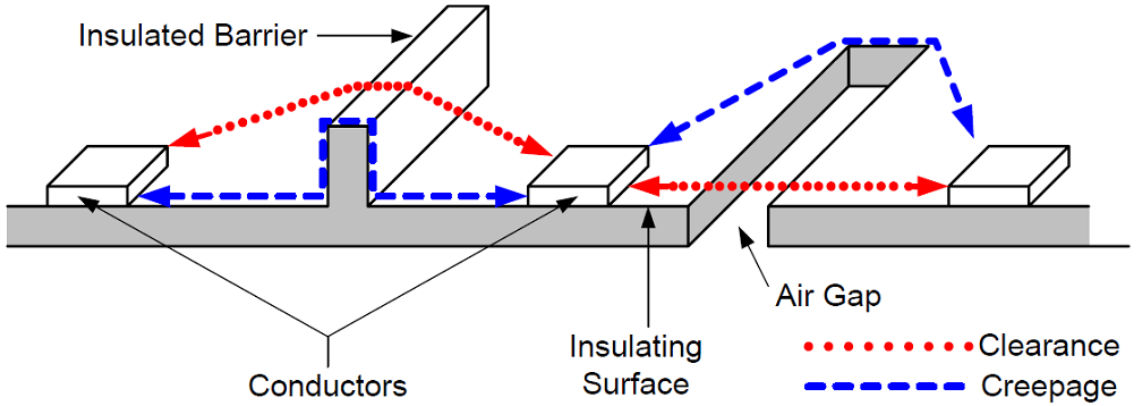




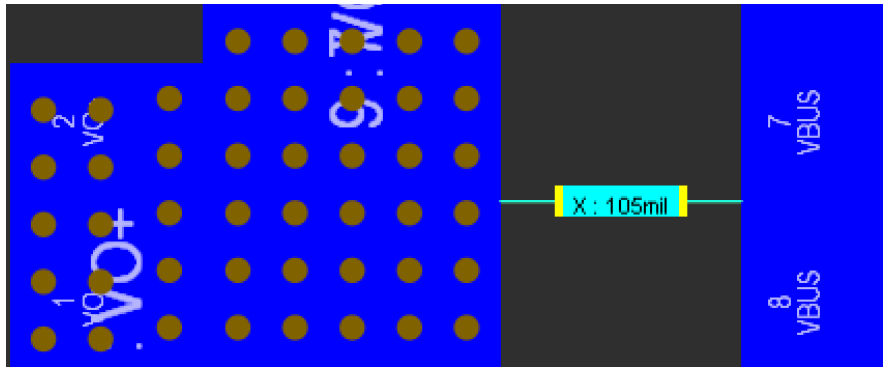




High Voltage Clearance



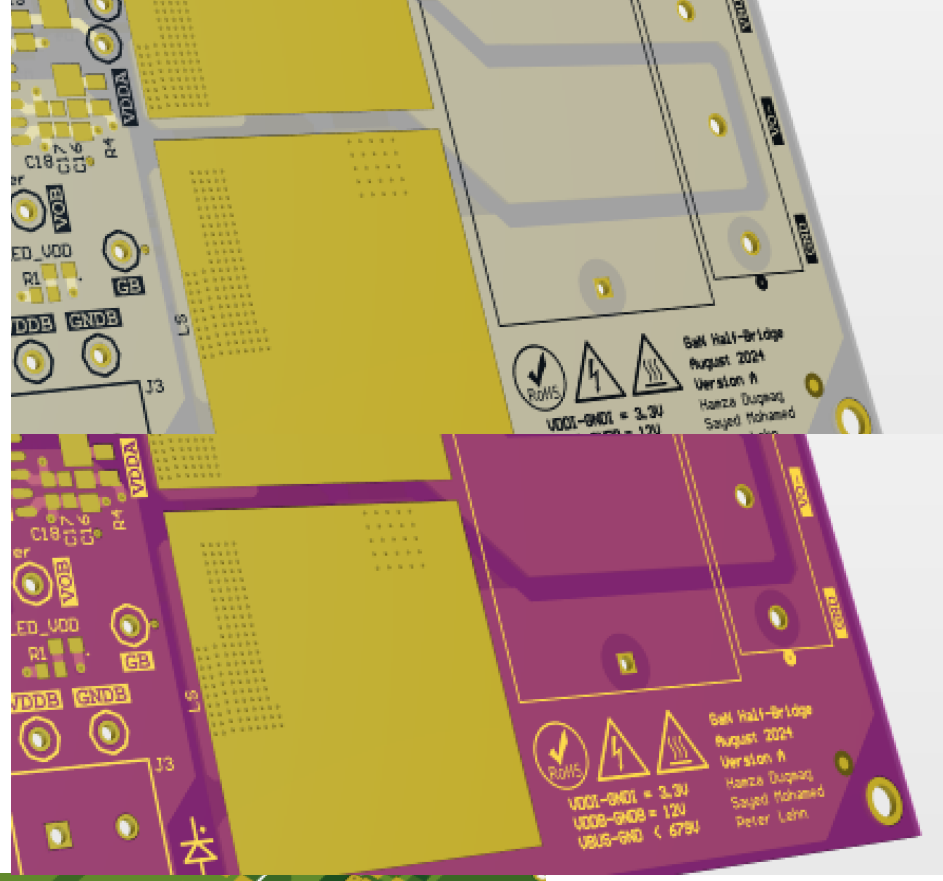
- IPC-2221 standard
- Power traces: design for 750V as a 10% FOS
- Challenge: maintain clearance while keeping layout compact and adding test points
  - Spent most time on this!
  - Iterated through layout ideas in design reviews
- Sanity check: DFN drain-to-source clearance:

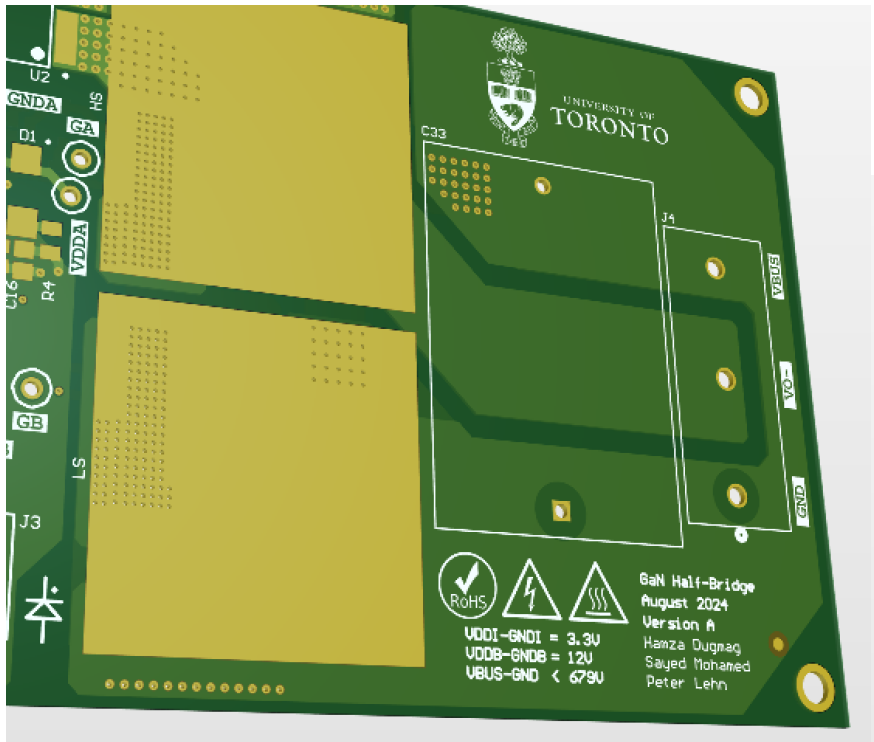


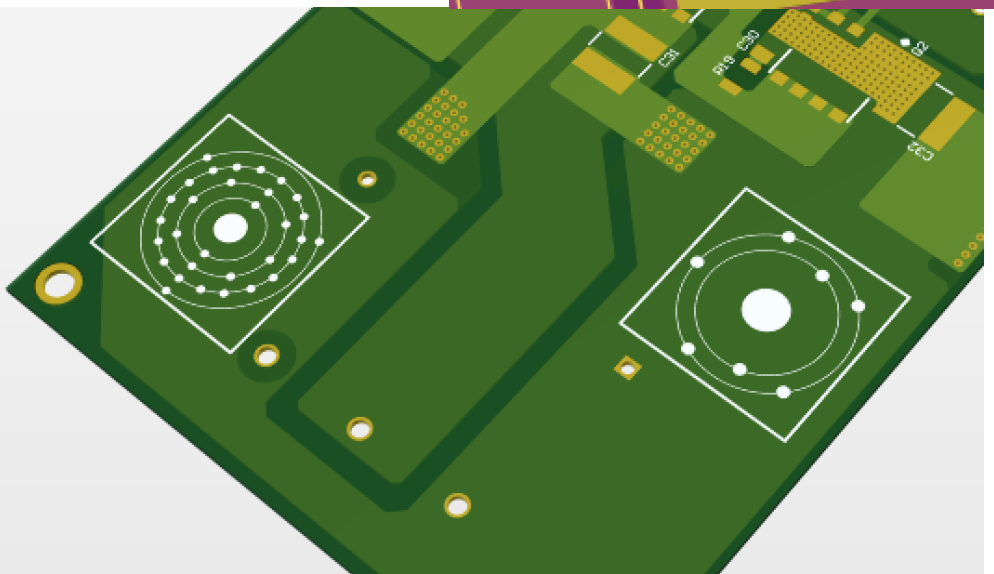
Voltage (DC or AC peak)	750	
Calculate		
SPACING	**mm**	**inches**
IPC-2221B:		
external	3.75	0.1476
internal	0.875	0.034
coated	1.56	0.0614
IPC9592	4.35	0.1713
Reset		

Silkscreen

- PCBs are a piece of art!
- White silkscreen + green solder mask
  - Best looking and ↑ fabricator capabilities







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Fabrication

PCB Order

- 5 boards from *PCBWay*:
  - DFM rules for *Altium*
- S1000H TG150:
  - ↑ Thermal stability, ↑ CAF resistance, ↑ Mechanical strength, etc.
- Time constraint:
  - 1oz Cu: still supports 5A
  - No assembly
- 4-layer stackup: >3kV

2 **4-layers PCB** Regular

Thickness: **1.6MM** Finished Outer Copper: **1OZ**

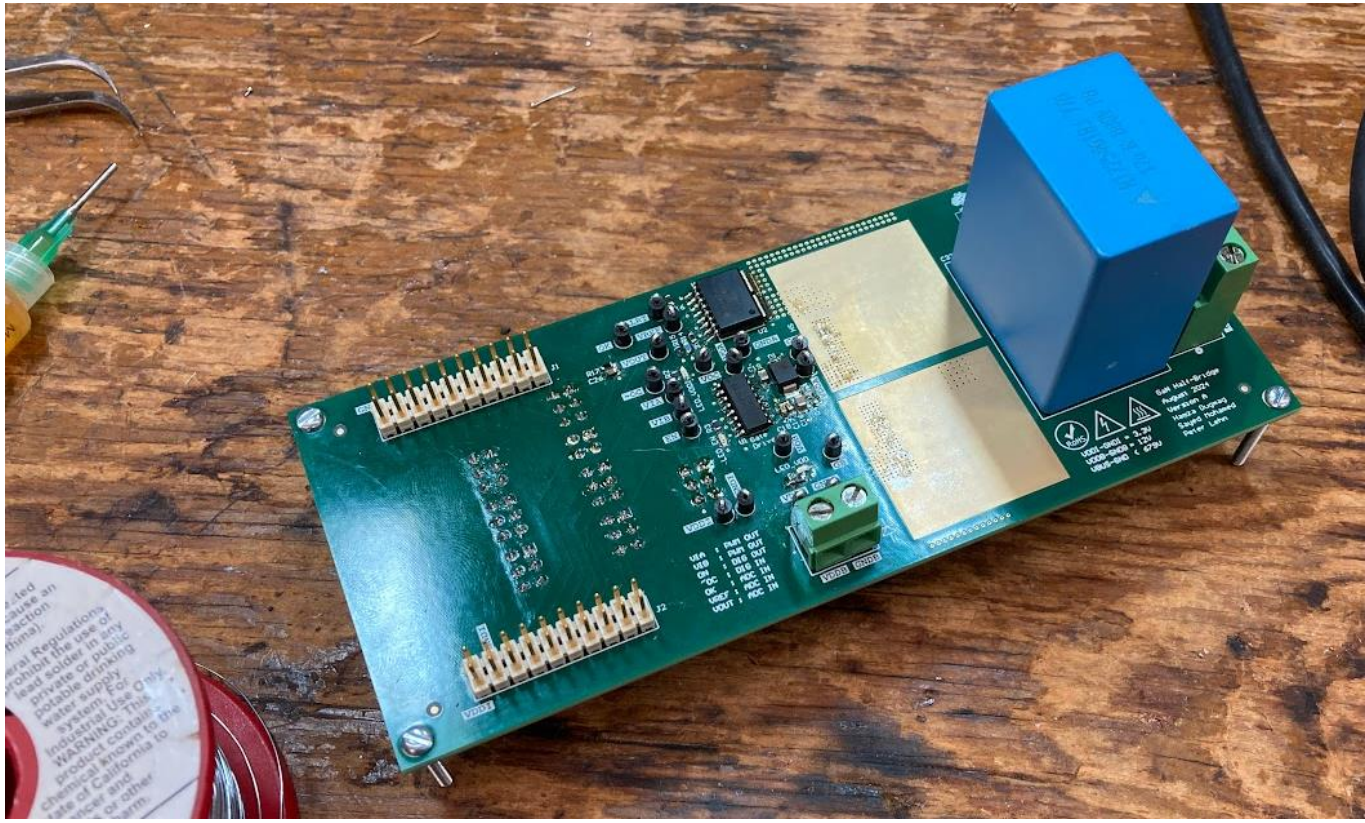
Inner Copper: **1OZ** Inner layer Residual copper ratio: **50%**

Layer	Material	Thickness (mm)	Thickness after lamination(mm)
L1-CU	Outer Base Copper 0.5OZ	0.0175	0.0175 (Plating to 1OZ)
PP	7628 RC46% DK:4.74	0.1960	0.1785
L2-CU	Inner Copper 1OZ	0.0350	1.1 (Core with Cu)
CORE	Core DK:4.6	1.0300	
L3-CU	Inner Copper 1OZ	0.0350	
PP	7628 RC46% DK:4.74	0.1960	0.1785
L4-CU	Outer Base Copper 0.5OZ	0.0175	0.0175 (Plating to 1OZ)

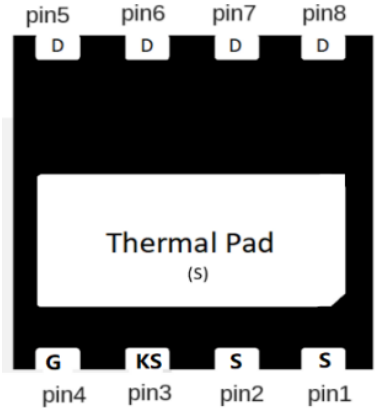
* Thickness after lamination: 1.49mm, tolerance: ±10%
* Finished PCB Thickness: 1.59mm, tolerance: ±10%
* 40% < Inner layer Residual copper ratio ≤ 60%, it is suitable to choose a lamination structure with 50% inner layer Residual copper ratio.

Soldering

- No access to reflow oven ☹
  - Not worth using stencil
- Manual through-hole and SMD soldering
- Challenge: heating large C_{DCL} and C_{sn} pads
  - ↑ Temperature
  - ↑ Time
  - ↑ Flux



DFN Soldering



- Thermal pad + huge heatsink area:
  - Solder paste + hot air gun + preheater
- Challenge: solder leaking through vias

Hand Soldering/Desoldering

GaN Systems

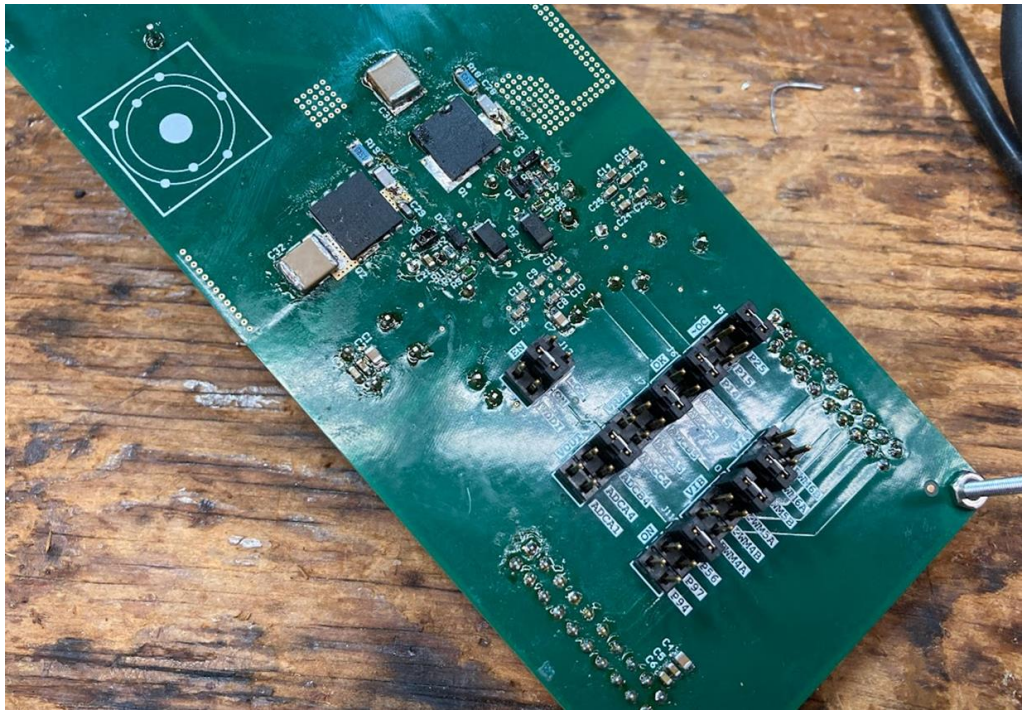
This slide shows recommended procedures for hand soldering/desoldering.

Hand soldering:

1. Attach a thermocouple close to the device pads for temperature monitoring.
2. Apply solder paste and flux to all the pads on the PCB. Alternatively, the pads can be pre-tinned using standard solder with solder flux added after pads are tinned.
3. Place the device on the board and align it properly.
4. Preheat the board to about 100-120°C using pre-heating station or hot plate. Apply a small force on top of the device to hold it down and use hot air gun to blow hot air from the top until the temperature reaches 260-280°C. Apply heat for 20-30 seconds.
5. Remove the force and heat.
6. Clean excess flux after it has cooled.

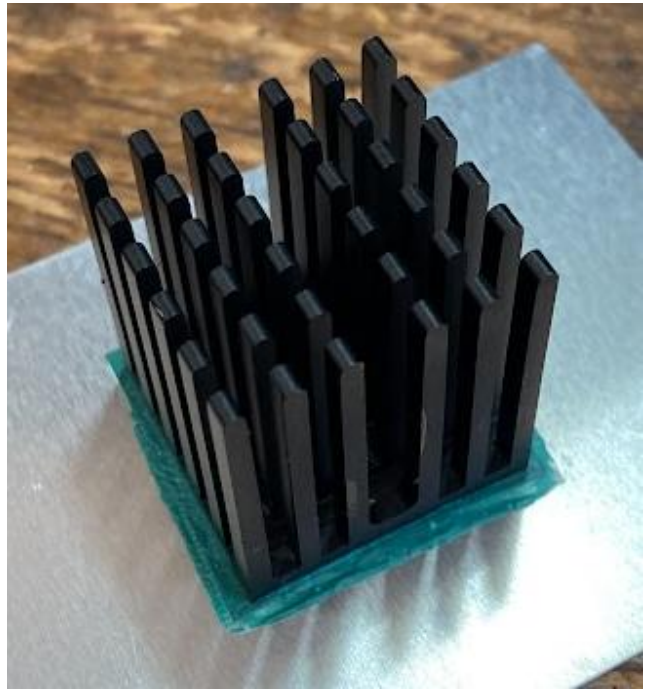
Desoldering:

1. Preheat the board to 100-120°C using a pre-heating station or hot plate.
2. Use a hot air gun to blow hot air at 260-280°C. Use tweezer to remove device once it is loose.



Heatsinks

- 55°C phase change TIM
  - Hot air gun to heat
  - Solidifies and adheres to pad and heatsink



Testing on bare aluminum piece

Verification

- Digital multimeter and inspection
- Continuity checks:
  - Proper connections
  - No solder bridges
  - TIM isolation
- Diode checks:
  - Correct polarity
- Resistance measurements

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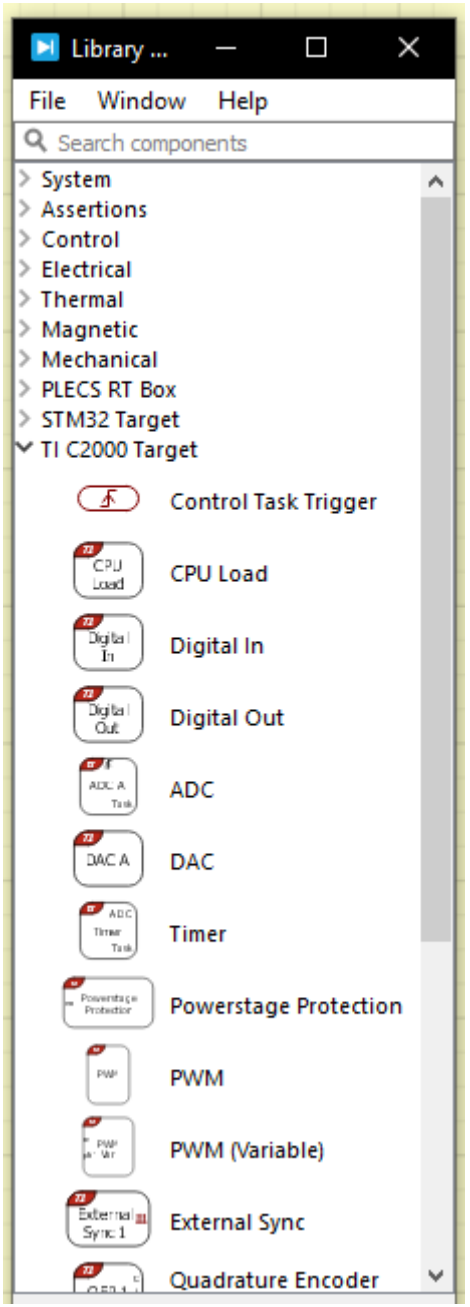
Firmware

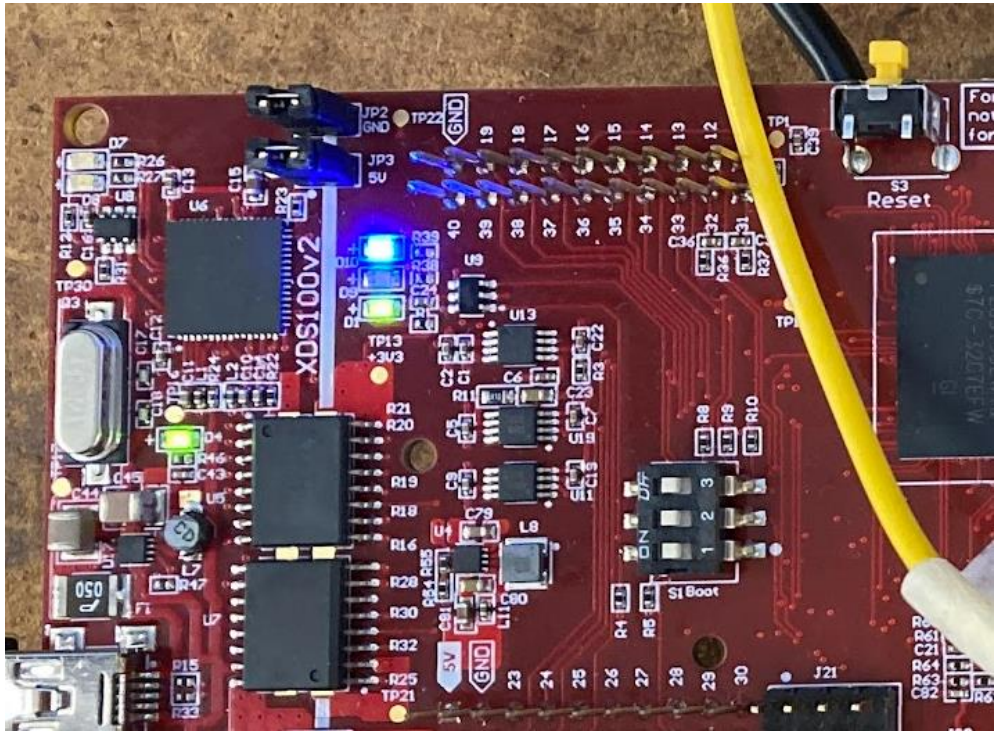
PLECS

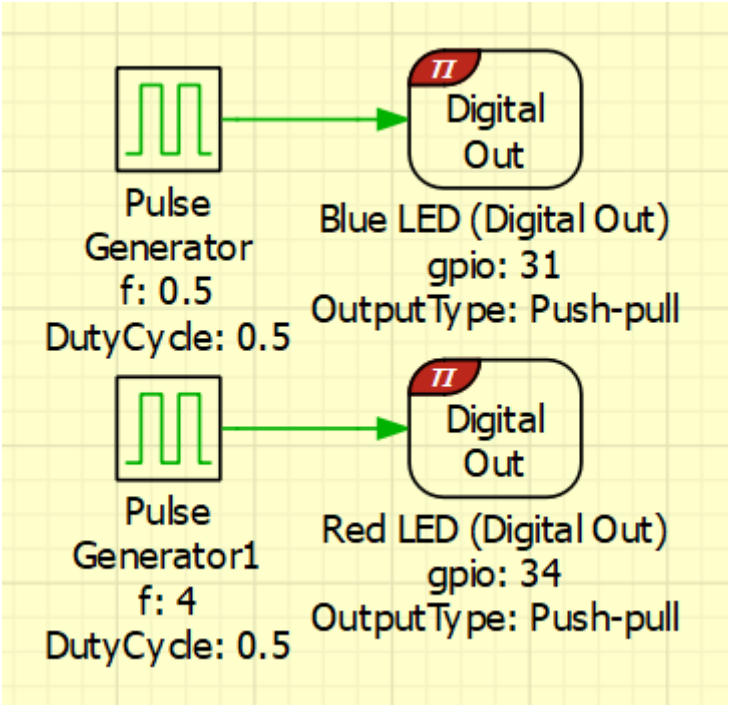
- Primarily for power electronics simulation and control
- Block-based programming
  - C2000 software development kit
  - Automatic code generation



LED Indicators

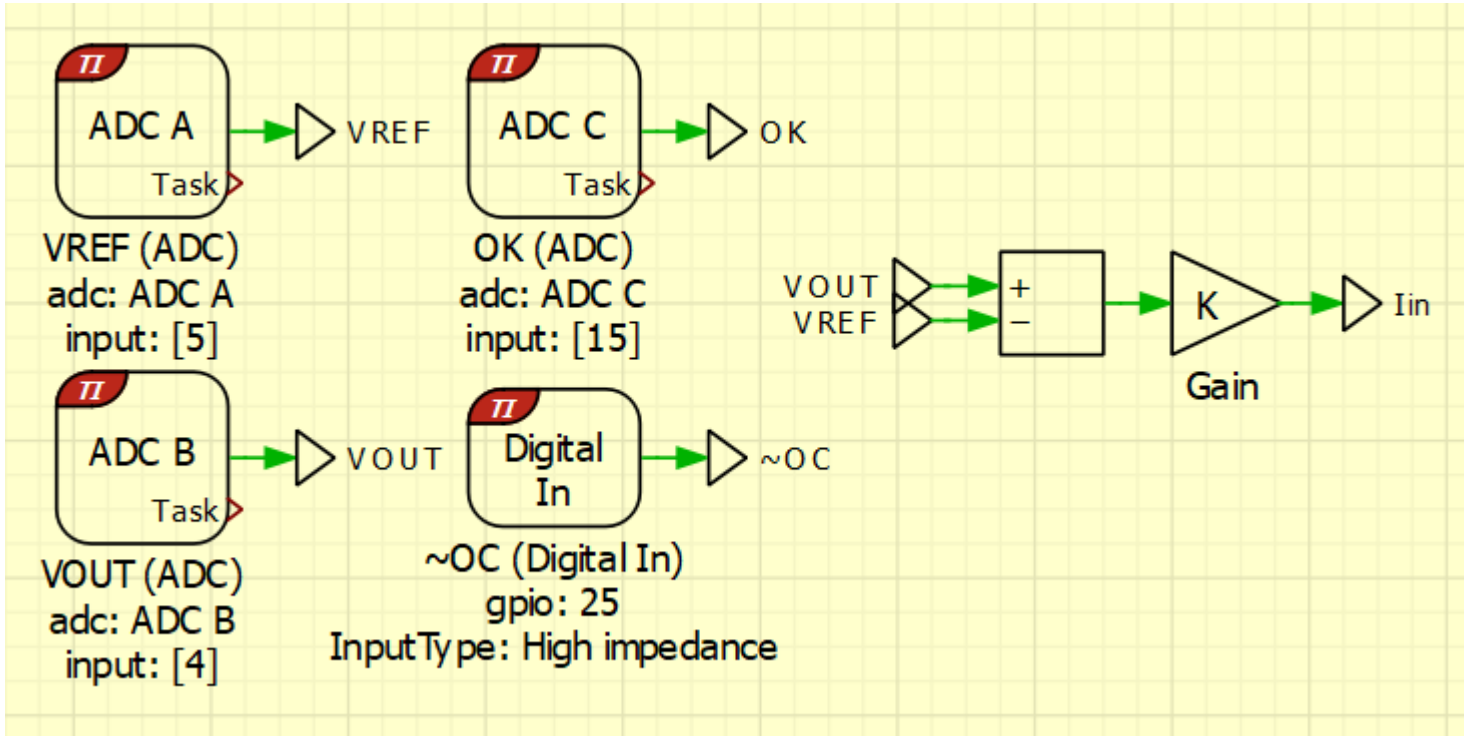
- Indicate flashing is complete and DSP is running





Hall Sensor ADC

- Calculate output current



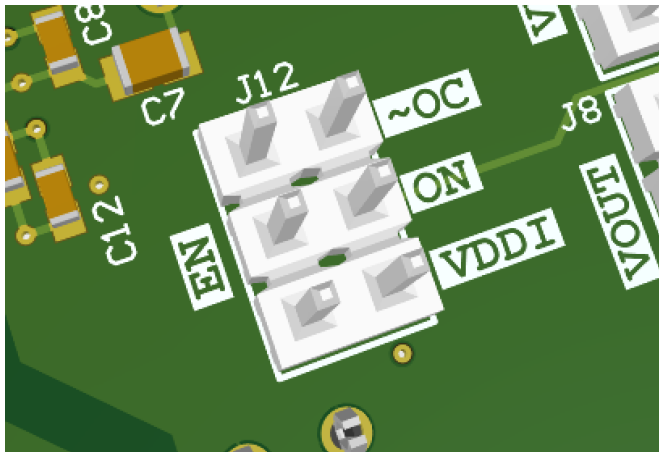
$$V_{OUT} = (I_{IN} \times S) + V_{REF}$$

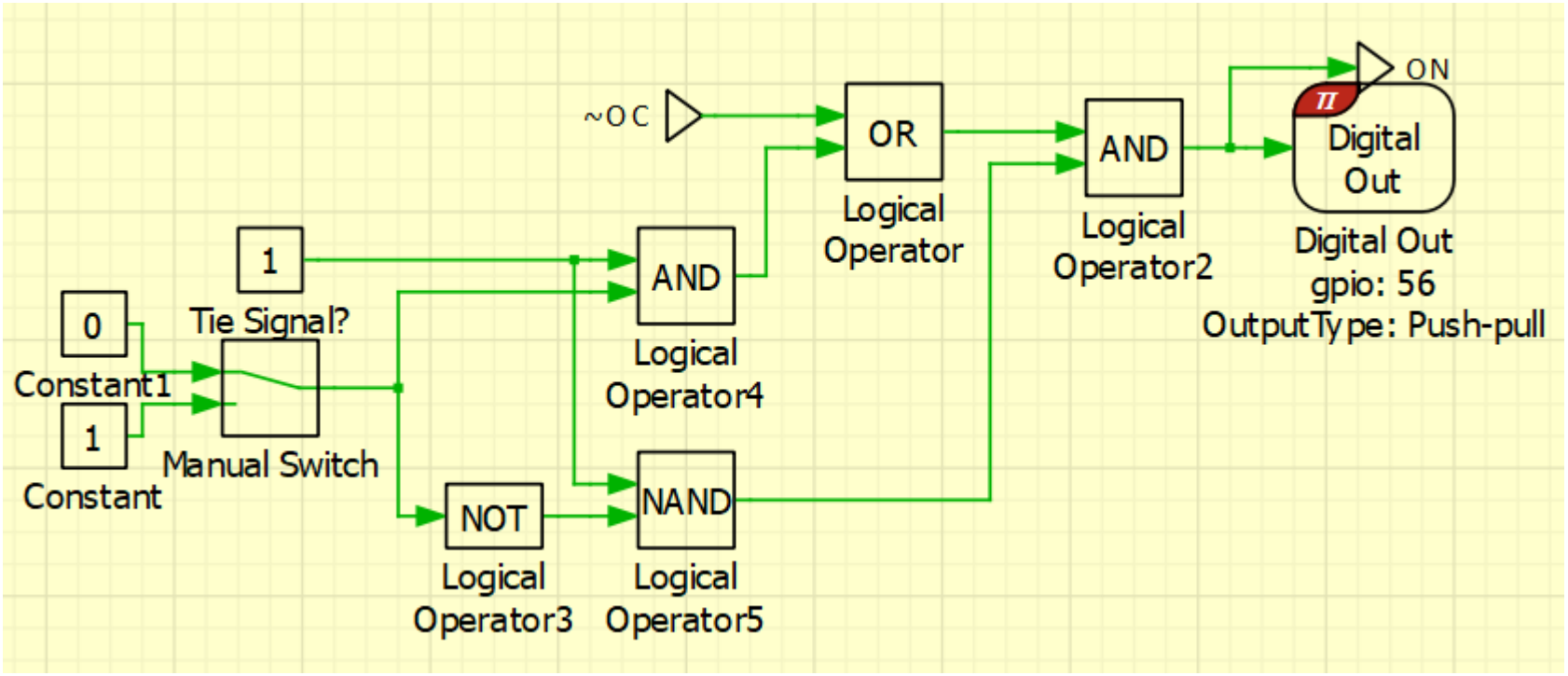
where

- V_{OUT} is the analog output voltage.
- I_{IN} is the isolated input current.
- S is the sensitivity of the device.
- V_{REF} is the zero current reference output voltage for the device variant.

Gate Driver Enable

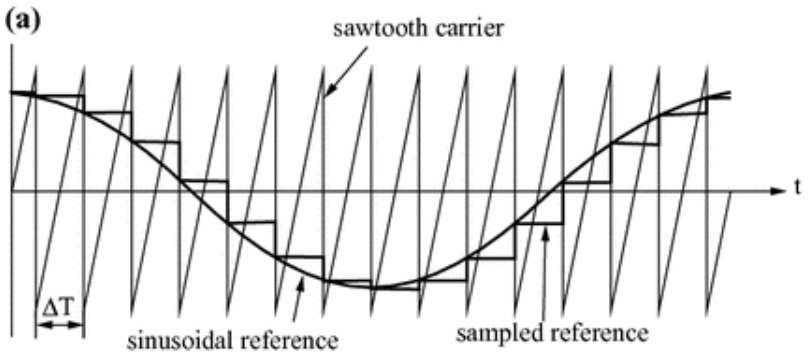
- Manual enable or tie to ~OC:
  - Former is done with switch while DSP is connected

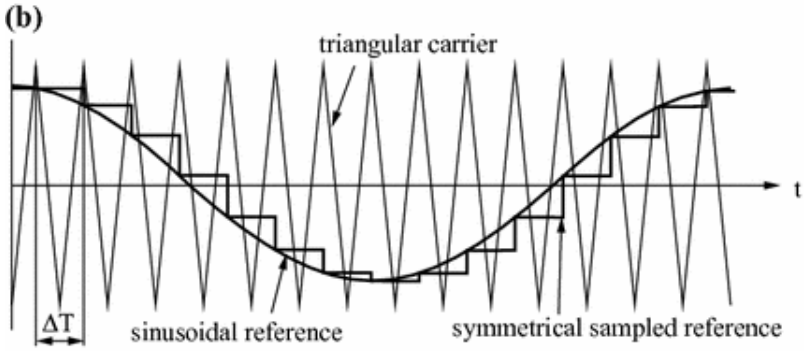


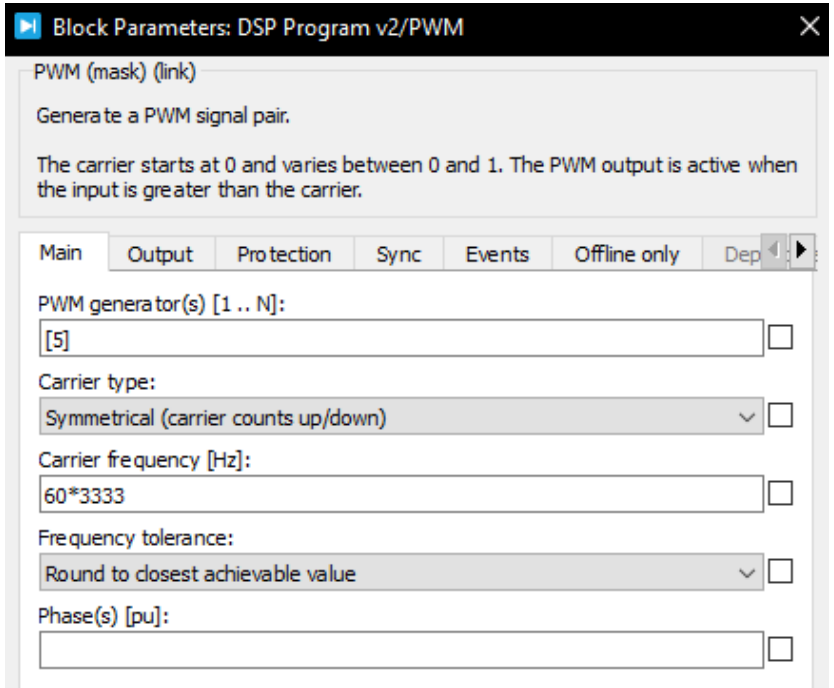


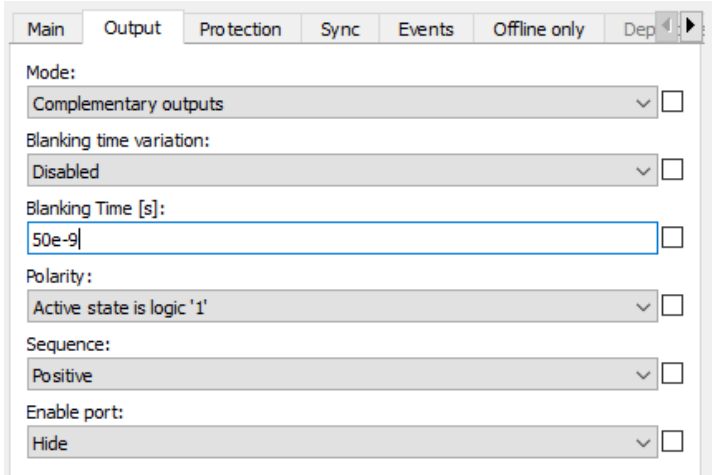
PWM Signal

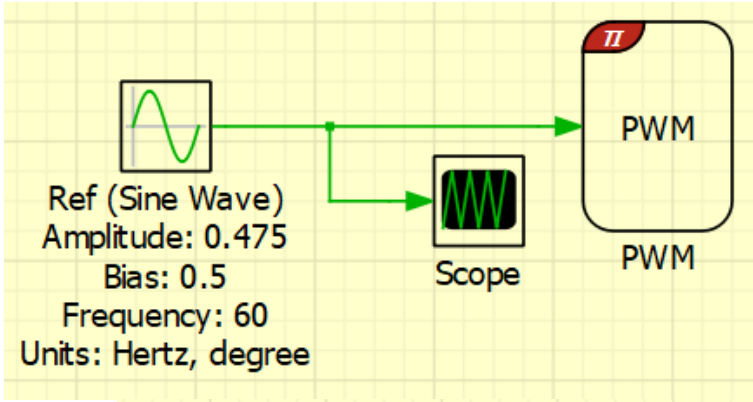
- Symmetrical carrier → better harmonics
- Complementary output
- Settable frequency and dead time

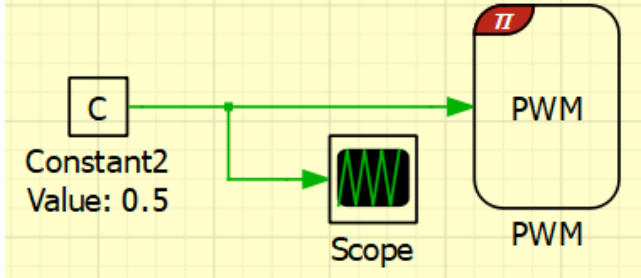






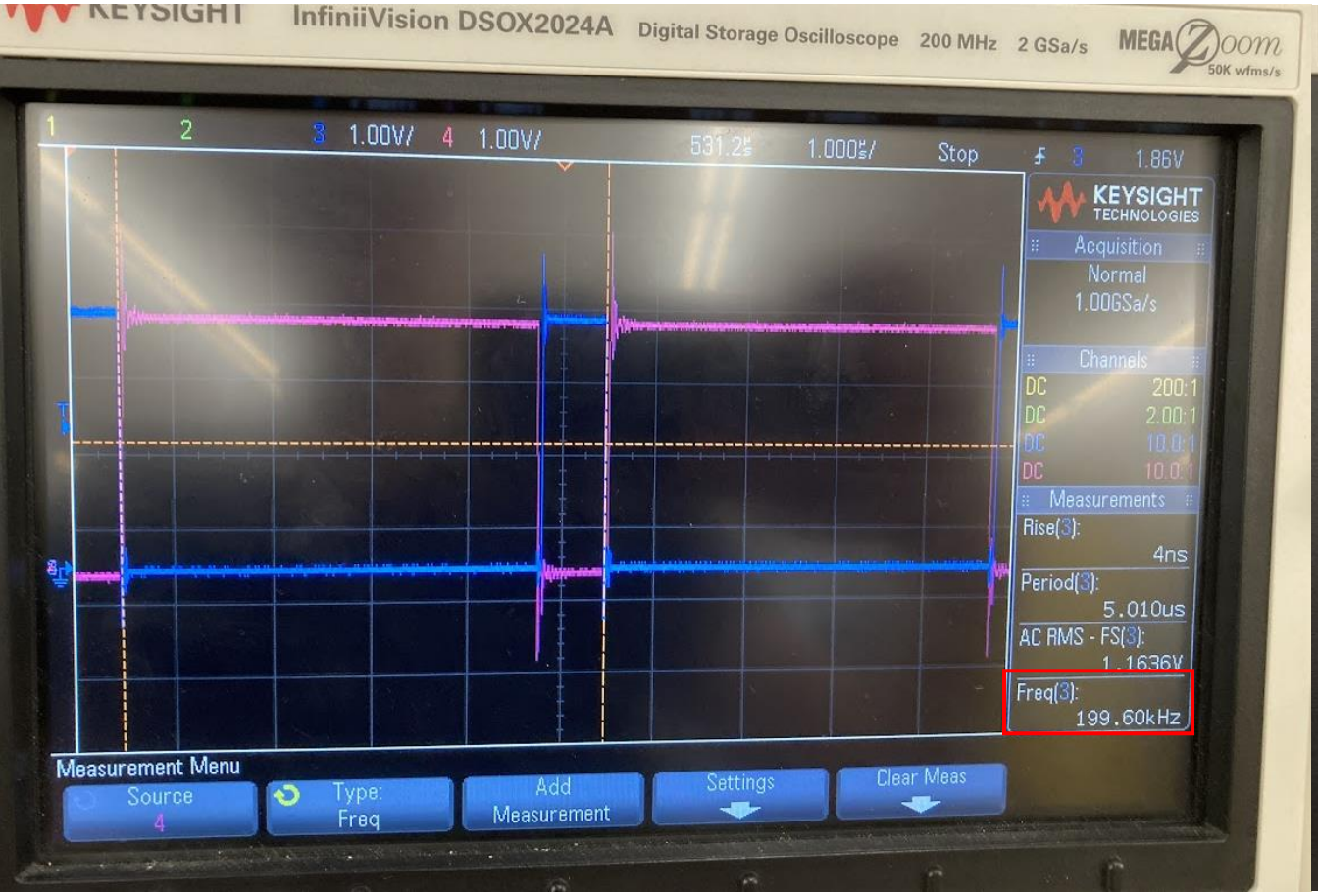






PWM Verification

- Confirm dead time and frequency



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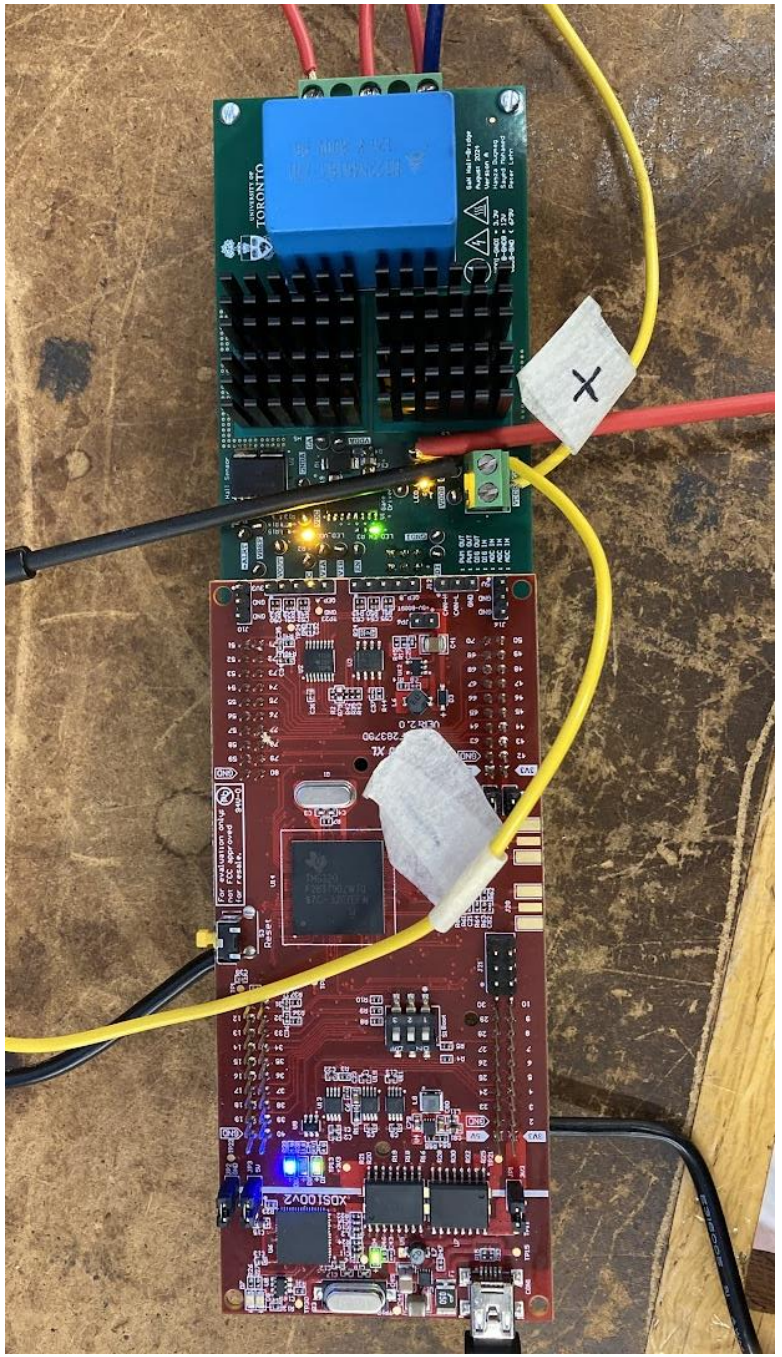
Testing

Validation Objectives

1. Open loop
2. Gate driving:
   - Driver IC
   - Bootstrapper
   - Level-shifter
3. Modulation (constant duty, SPWM, dead time)
4. Oscillations and spikes
5. Filter and output

Testing Strategy

1. Connect DSP (orange LED 1)
2. Flash firmware (start at $\downarrow V_{bus}$, $\downarrow f_{sw}$, $\uparrow T_{dead}$)
3. Power gate driver (orange LED 2) and DC bus
4. Enable gate driver (green LED)
5. Disable gate driver
6. Change parameters and re-flash
7. Repeat 4-6



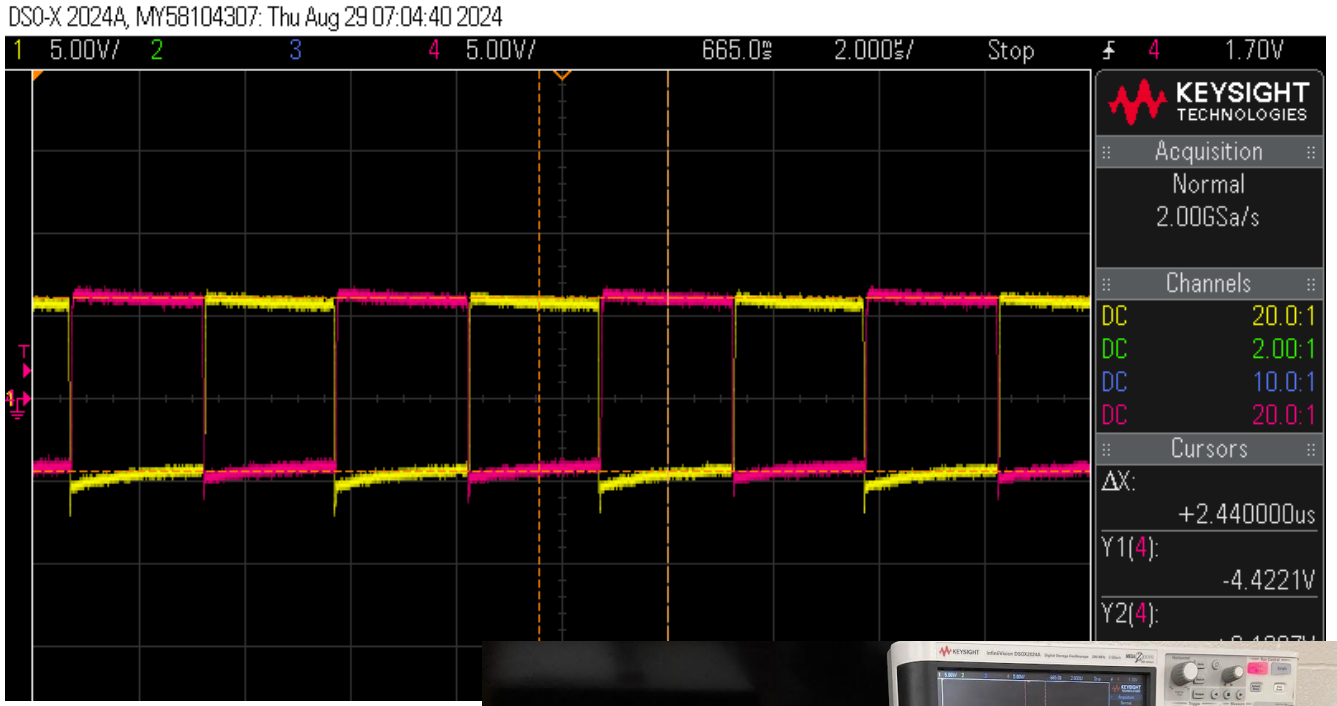
Equipment and Probing

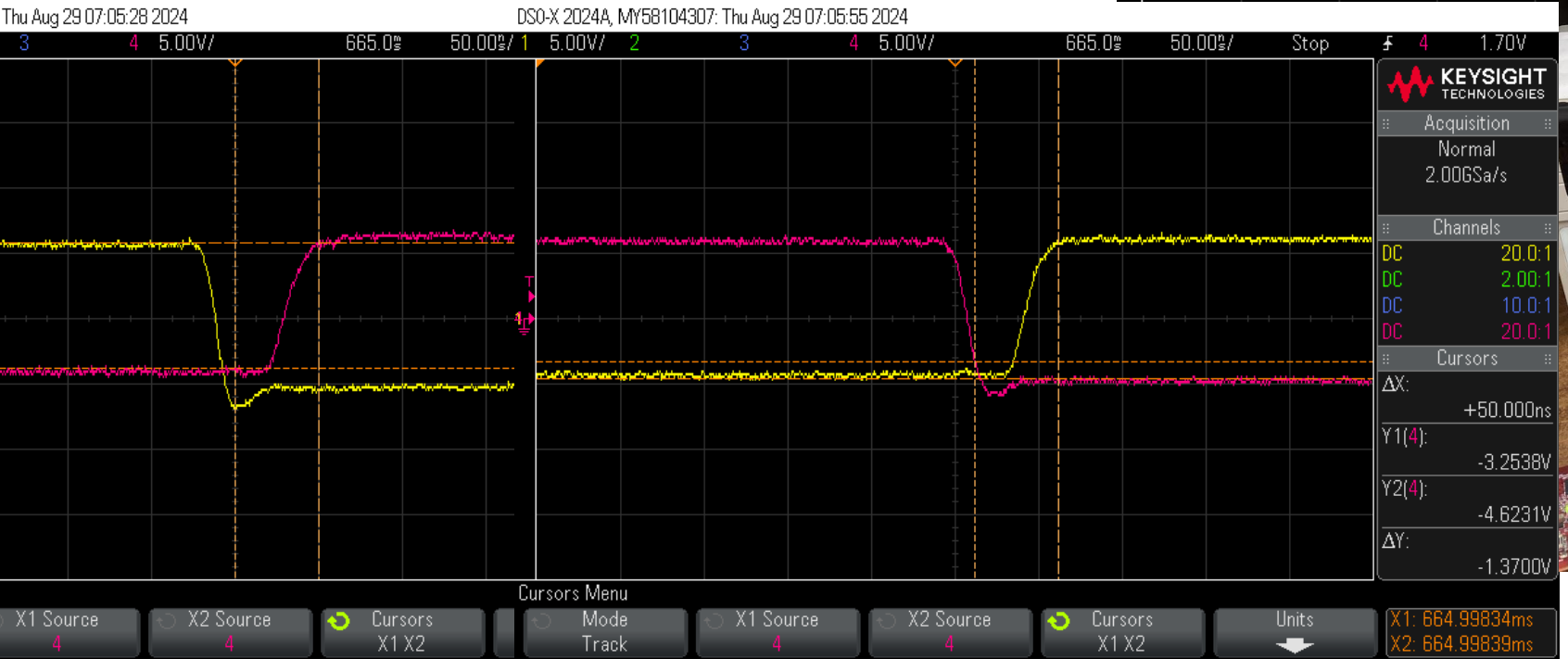
- Digital oscilloscope
- Isolated power supplies:
  - <10kW for HV bus
  - <30V for gate driver and LV bus
- High signal-bandwidth probes:
  - Differential voltage
  - Current clamp
- Thermal camera

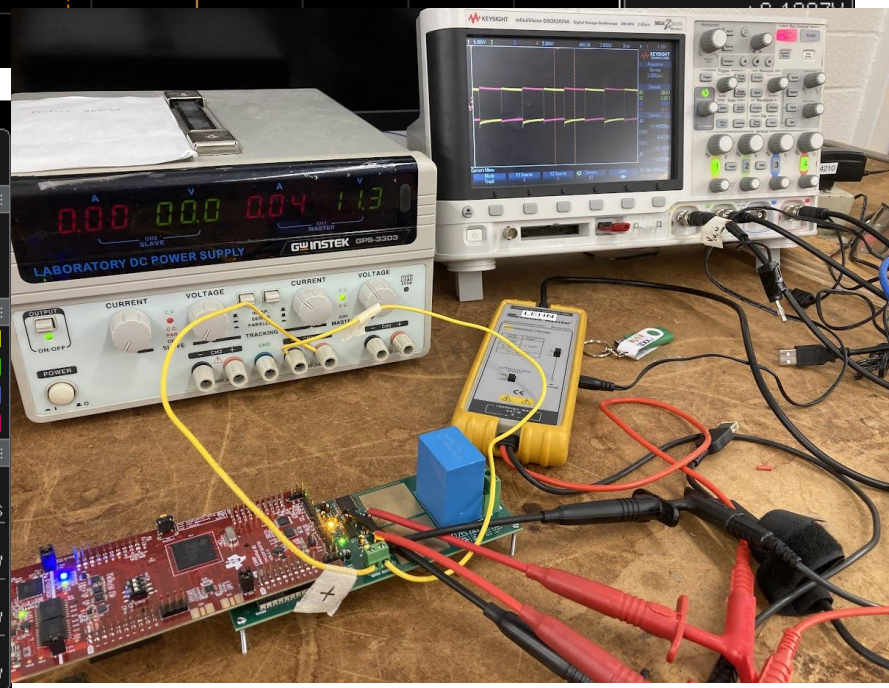
$V_{gs,low}$
$V_{gs,high}$
V_{sw}
V_{load}
I_L

Test #1: Gating

- Gate driver and level-shifting
- No load, 200kHz, 50ns DT
- Undetectable Miller plateau

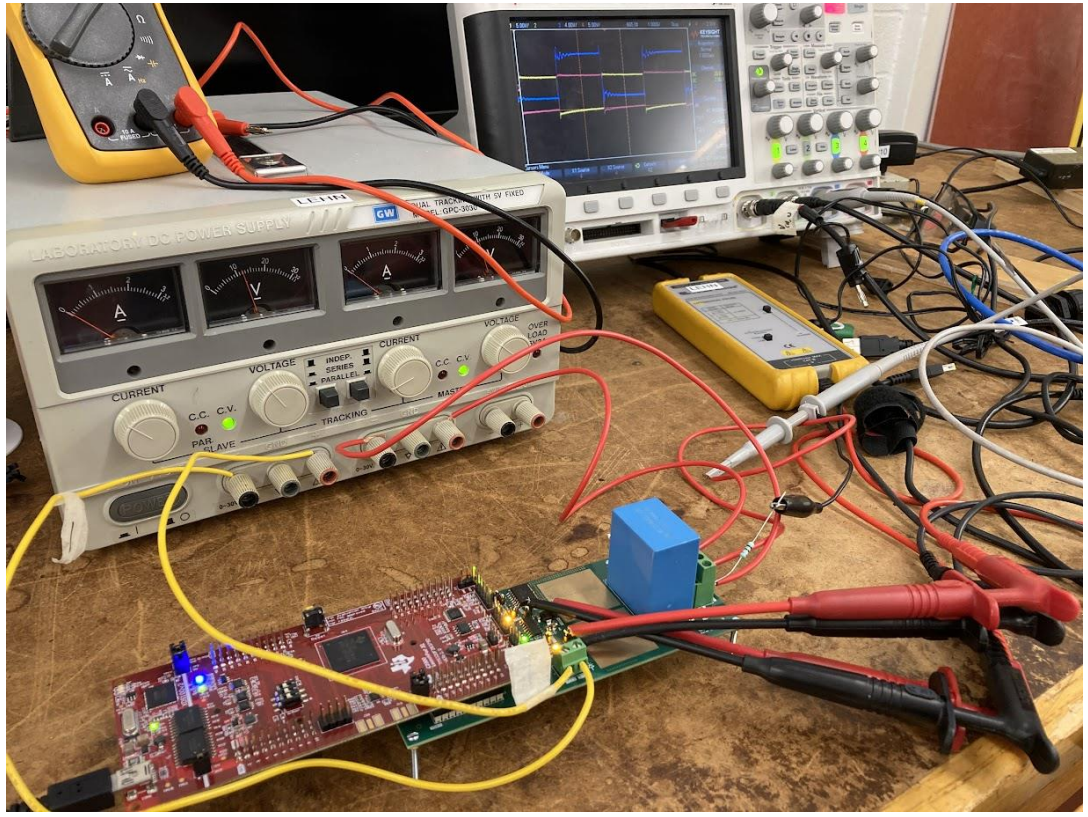


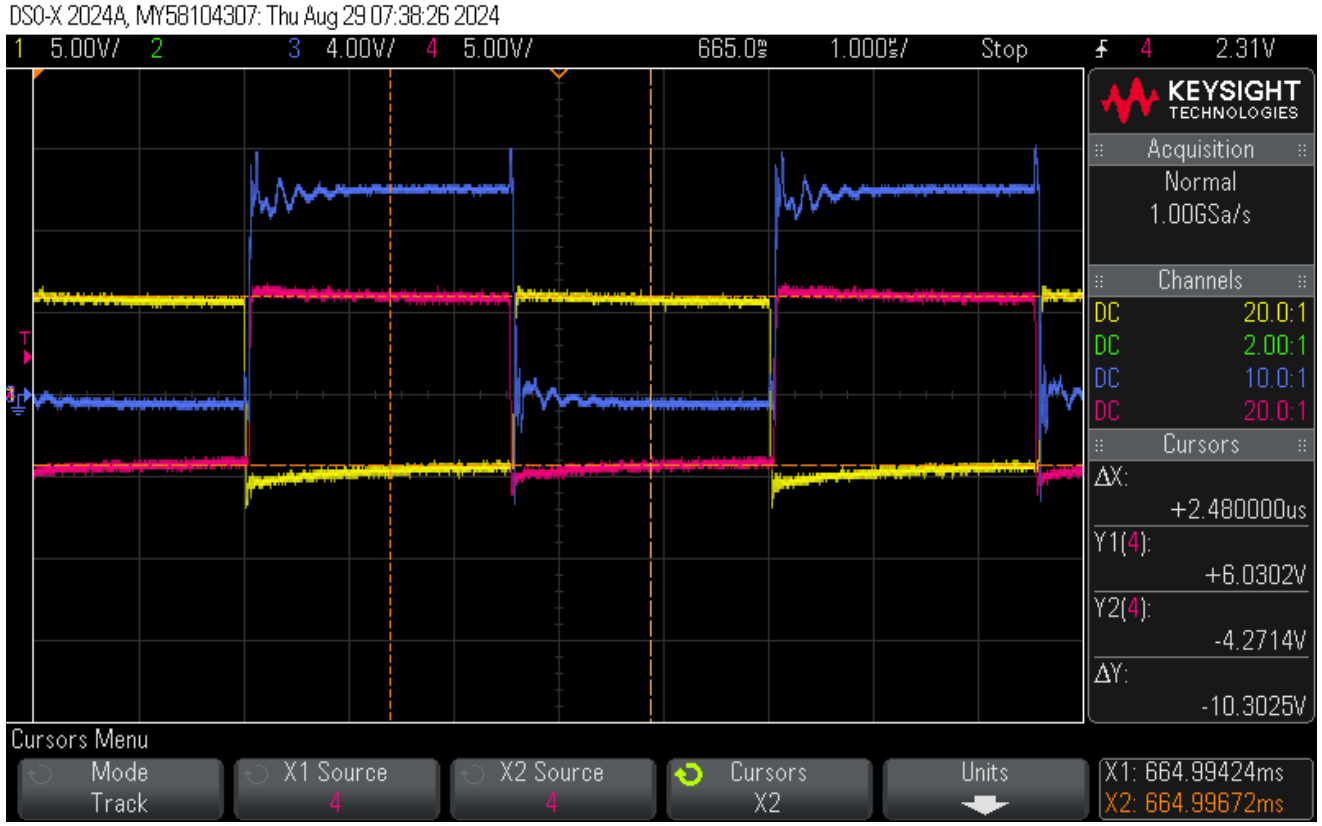




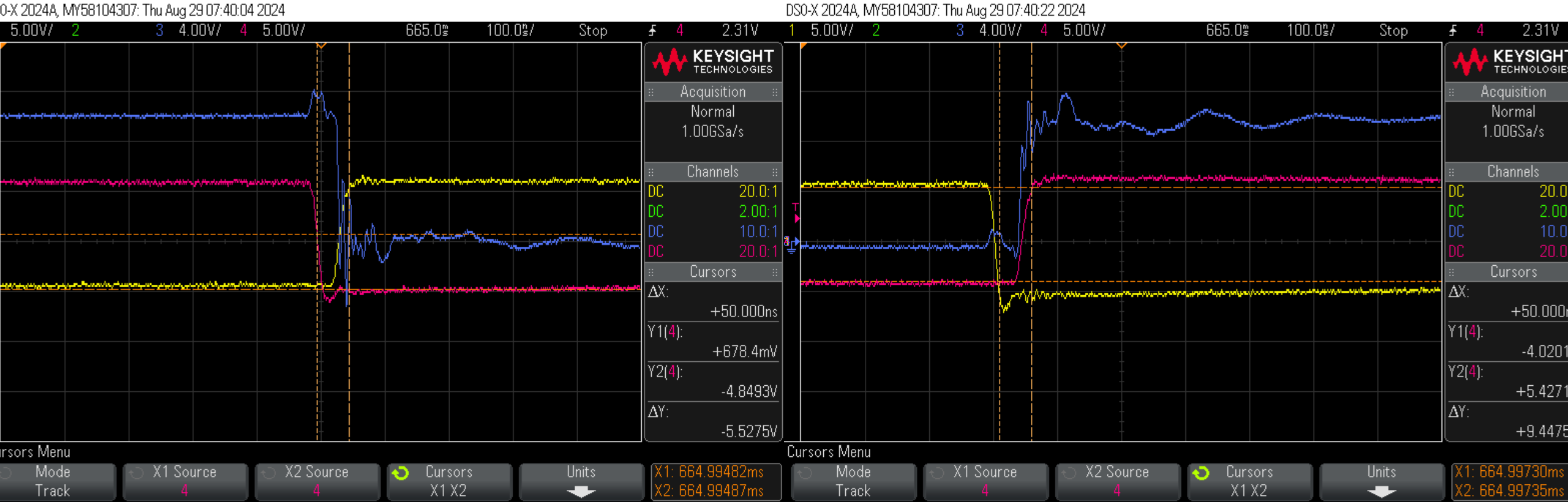
Test #2: Switch Node

- 10V bus, no load
- Some ringing



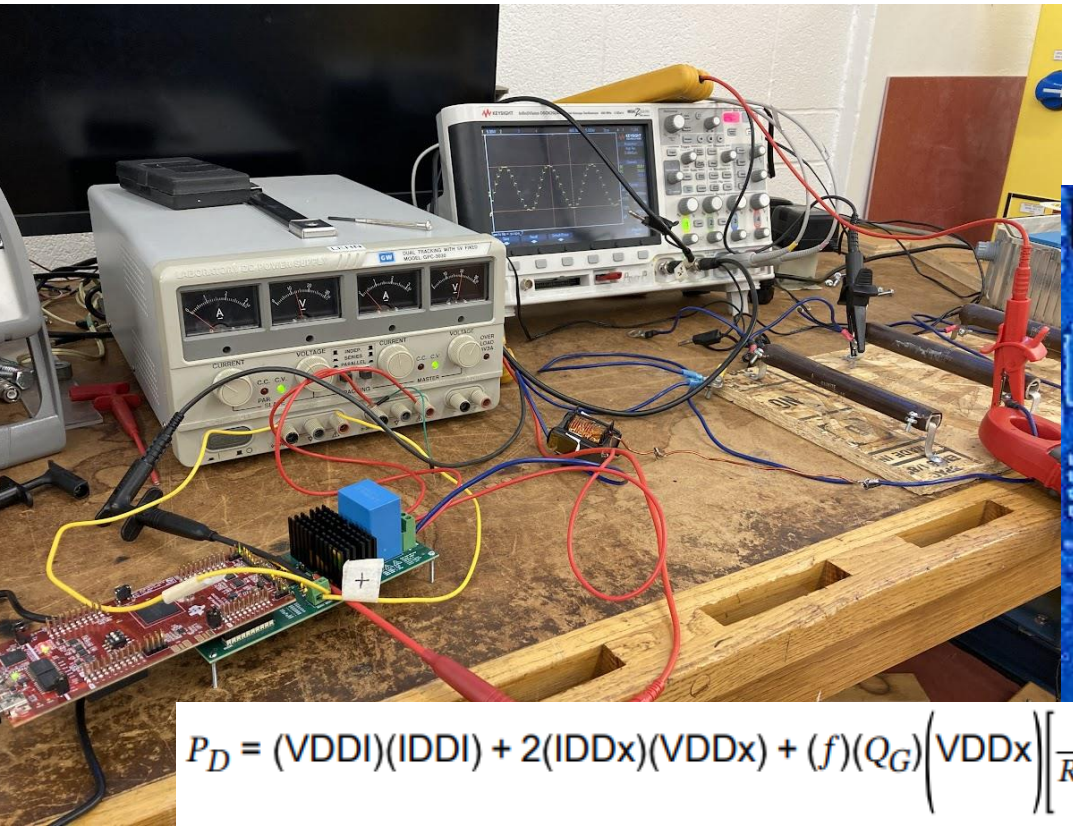


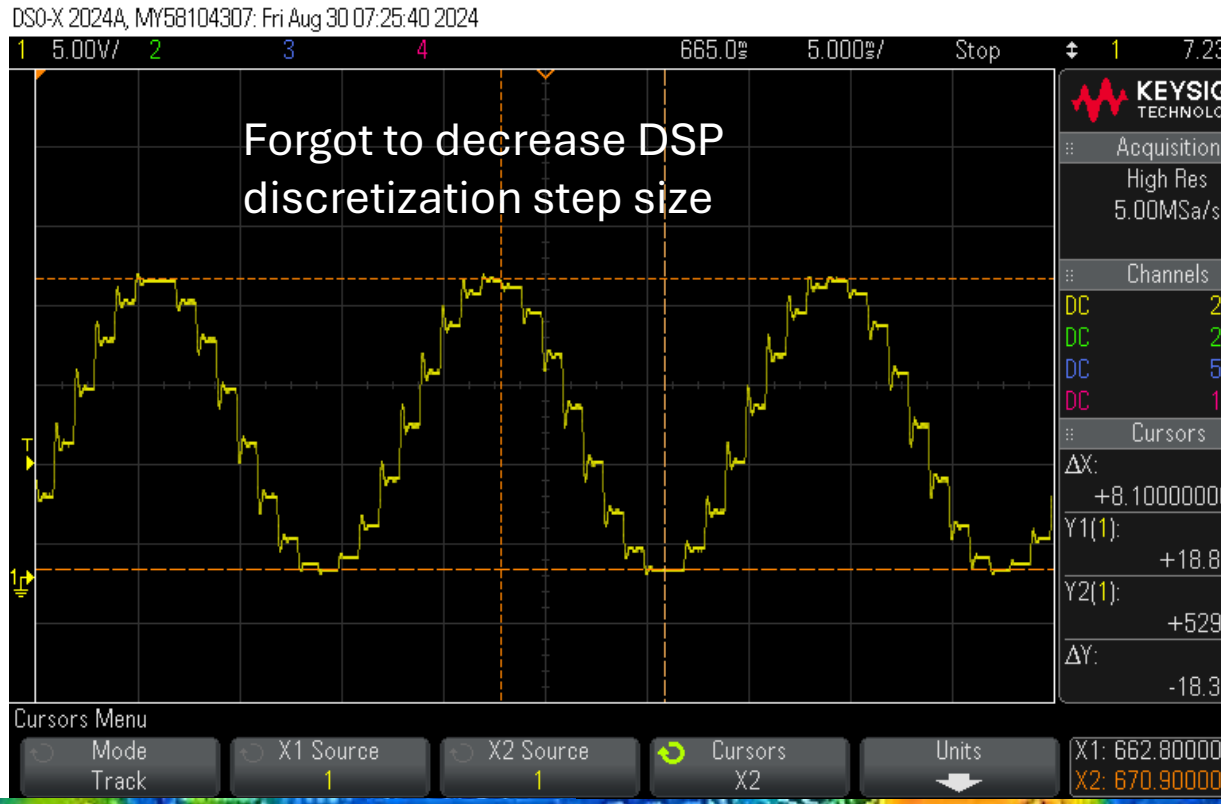
Test #2: Switch Node

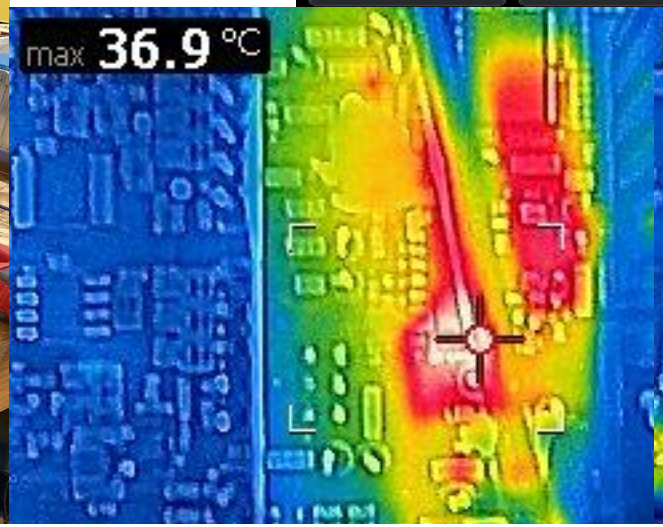


Test #3: SPWM

- 20V, 0.55mH, 10µF, 25Ω 100W
- Gate driver hotter than switches



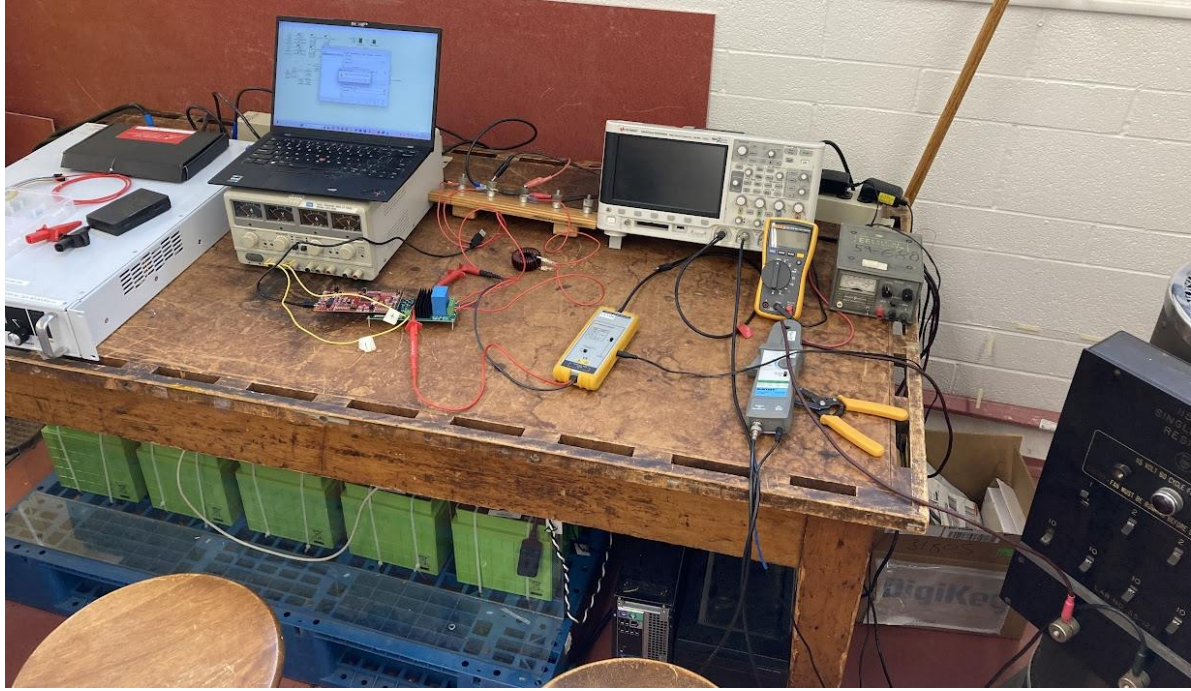


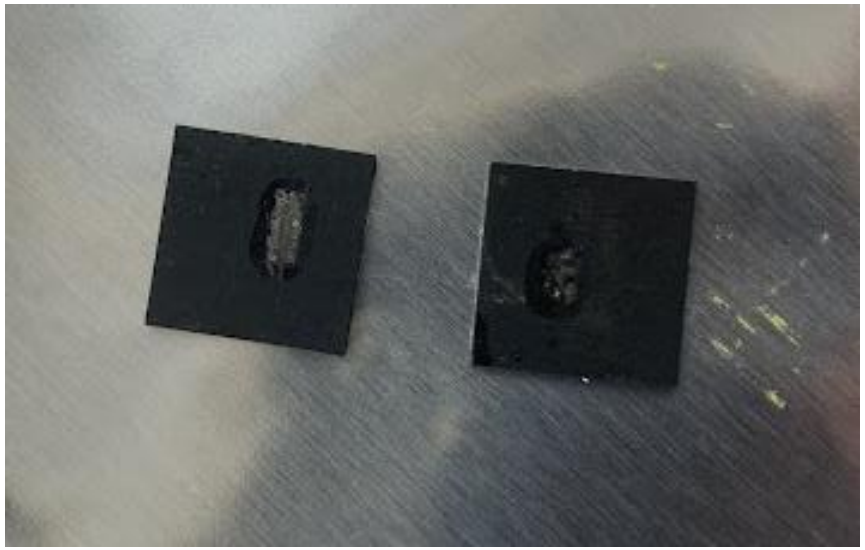


$$P_D = (\mathrm{VDDI})(\mathrm{IDDI}) + 2(\mathrm{IDDx})(\mathrm{VDDx}) + (f)(Q_G)\left(\mathrm{VDDx}\left[\frac{R_P}{R_P + R_G}\right] + \left(f\right)\left(Q_G\right)\left(\mathrm{VDDx}\left[\frac{R_N}{R_N + R_G}\right] + 2fC_{\mathrm{INT}}\mathrm{VDDx}^2\right.\right.$$

Test #4: Stress Test

- Constant duty cycle (sync. buck)
- Trial #1: 600V 3A 100kHz 150ns DT
- Trial #2: 700V 2A 100kHz 150ns DT
- Failure analysis:
  - ~40 °C, ∴ not thermal
  - Open-circuit, ∴ voltage breakdown
  - Voltage spikes from parasitic inductances





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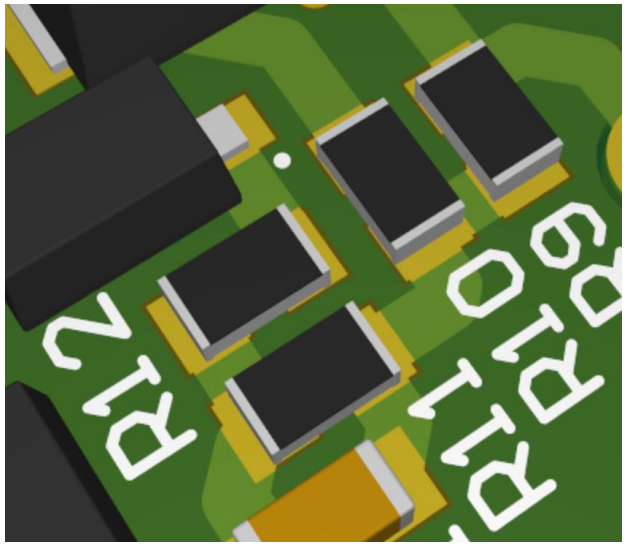
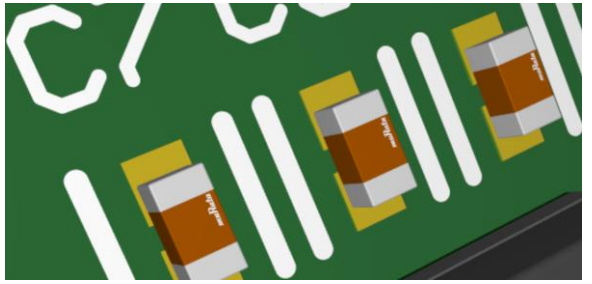
Conclusion

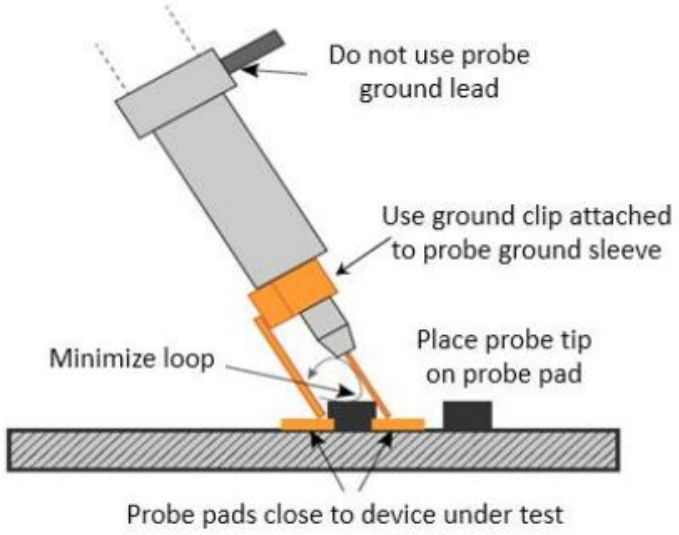
Improvements

- Further mitigate parasitic inductances
  - Explore different layouts (more compact and fewer vias)
  - Design snubber experimentally
- Silkscreen border around components
  - Prevent soldering mistakes
- Explore TIM alternatives
  - Avoid phase change at 55 °C
  - Heatsink spring clips
- Probe LS gate with short ground clip
  - Minimize probe loop inductance
  - Mitigate any influence on system performance



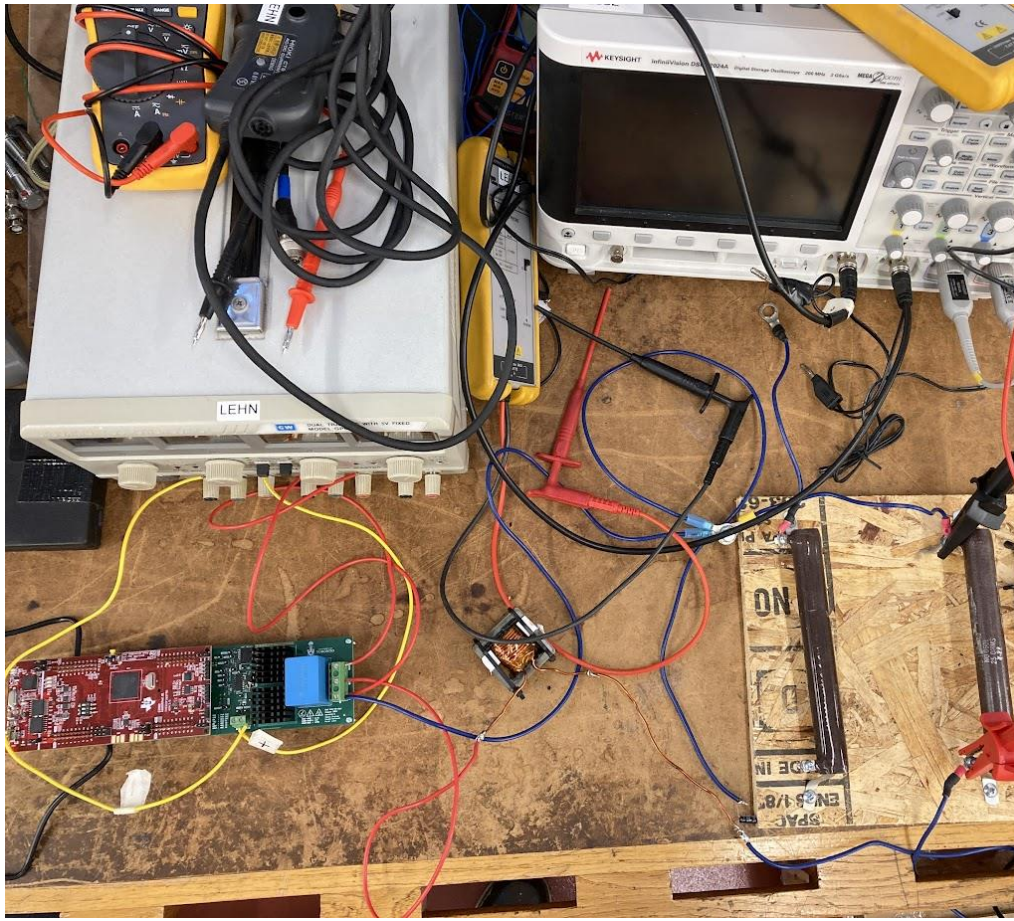
vs.





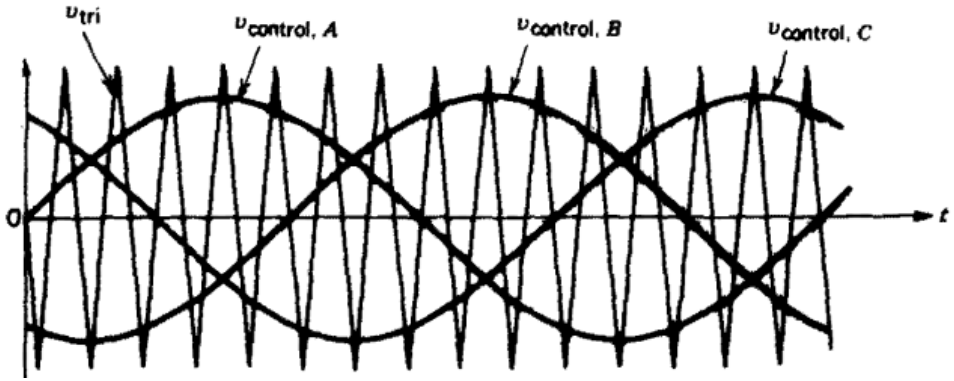
Outcome and Achievements

- GaN synchronous buck converter
- Excellent gate driving at 100 kHz
- Learned a lot!
  - End-to-end ownership, making decisions, design review communication, collaboration, design iteration
- Completed exploration in half the planned time
  - 8 mo. → 4 mo.
  - Got most things working first try



Next Steps

1. Negative current testing
   - Idea #1: Operate as boost (risky!)
   - Idea #2: Full-bridge (gating sync!)
   - Idea #3: Center tap (capacitor ratings!)
   - Idea #4: Negative V_{bus}
2. Efficiency analysis (power analyzer)
3. Closed-loop control
4. Three phase inverter (with better layout)
5. PCB-stator PMSM test



Acknowledgements

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  - Supervision
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Questions?