Bidirectional-GaN Current Source Inverters for PCB-Stator Axial-Flux Permanent Magnet Synchronous Motors

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Supervisor: Peter Lehn

April 7, 2025

B.A.Sc. Thesis

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Abstract

Emerging axial-flux permanent magnet synchronous motors (AFPMSMs) with printed circuit board (PCB) stators offer efficiency, power density, and manufacturing cost benefits over traditional radial-flux motors. However, their low stator inductance makes it difficult to meet current ripple requirements, especially when driven by voltage source inverters (VSIs). This undergraduate thesis addresses this challenge by designing the first current source inverter (CSI) prototype using *Infineon*'s new 650 V 14 A monolithic bidirectional gallium nitride (GaN) switches (IGLT65R055B2). This aims to resolve the cost and efficiency challenges associated with CSIs to leverage their benefits as motor drives.

Our compact, four-layer PCB features a GaN-based synchronous buck DC current regulation stage, a 1.1 mH DC link inductor, negative turn-off gate driving circuitry, a 2.2 μF output capacitive filter, and a three-phase CSI designed for switching at 200 kHz. Controlled by a *Texas Instruments* C2000 digital signal processor, space vector pulse width modulation (SVPWM) for the CSI and hysteretic current control for the buck are implemented in *PLECS*.

The prototype was validated experimentally under low power operation ($\leq$ 30 V, 1 A) using a three-phase Wye-connected resistive load. The CSI successfully regulates the DC link current and outputs balanced sinusoidal output currents as confirmed by oscilloscope measurements. This validates the feasibility of leveraging these new reverse-blocking switches in an efficient CSI topology. Future work entails validating the prototype as a PCB-stator AFPMSM motor drive and characterizing the system's efficiency. Ultimately, this thesis highlights a promising path towards compact and efficient electric drives leveraging cutting-edge GaN technology.

Acknowledgements

I would like to express my sincere gratitude to Prof. Peter Lehn for his support, mentorship, and guidance throughout the year. I am also thankful to everyone in Prof. Lehn's group, especially Sayed Mohamed for his help with setting up my experiments in the lab and troubleshooting. This work could not have been made possible without Chatumal Perera and Meha Pathmanathan (*Celestica*) helping us get our hands on research samples of *Infineon*'s IGLT65R055B2 devices. Finally, I am thankful to Eric Persson (*Infineon*) for his expert advice and insights into how these devices work and how we can make the most out of them.

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Chapter 1

Introduction

1.1 Climate and Industry Contexts

The *Paris Agreement*, signed in 2016 by 195 countries, declares a long-term goal to maintain global average surface temperatures well below 2 °C above pre-industrial levels, preferably 1.5 °C at most [8]. Unfortunately, the current energy policy landscape and development suggests an average temperature increase of 2.4 °C by 2100 [9]. Also, 2024 has been the hottest year on record, exceeding 1.5 °C above pre-industrial levels for the first time [10, 11]. Although the 1.5 °C limit from the *Paris Agreement* is in the context of long-term global warming, which gives time for temperatures to drop back down, this outlook towards ever-increasing temperatures poses significant risks for the well-being of humans and ecosystems [9, 10]. Each year introduces a number of unprecedented weather events, including wildfires, droughts, heat waves, and floods around the world.

For decades, climate change has been driven by the fact that around 80% of the global energy mix consists of fossil fuels (coal, oil, and natural gas), with carbon dioxide emissions set to peak before 2030 at around 37 gigatonnes [9, 10]. Combating this requires electrifying the global energy economy and decarbonizing the power grids. From 2023 to 2035, the global electricity demand is estimated to rise by around 1000 TWh per year as overall energy demand increases and fossil fuels are being replaced [10]. Among other innovations, improvements in electric motor efficiency are increasing the appeal for electrification. Even when connected to a fossil fuel based grid, improving the efficiency of electric end-use devices contributes to reduced carbon emissions.

Electric motors compose more than half of the world's total electricity consumption across various sectors like buildings, agriculture, and industry [1]. In the latter, motors consume at least 70% of industrial electricity to drive pumps, fans, and other processing systems for sub-sectors like chemicals, food, and metals and textiles [1]. Depending on the scale of processing, their power outputs range anywhere from less than 0.1 kW to 1000s of kW [1]. To control electricity consumption, policy-makers have prioritized enforcing minimum energy performance standards (MEPS) on the motor [1]. Almost 90% of global industrial motors are covered by MEPS, and around 45% of the total saved energy from 2000 to 2021 due to energy efficiency measures (125 exajoules) are because of MEPS for industrial electric motors [12].

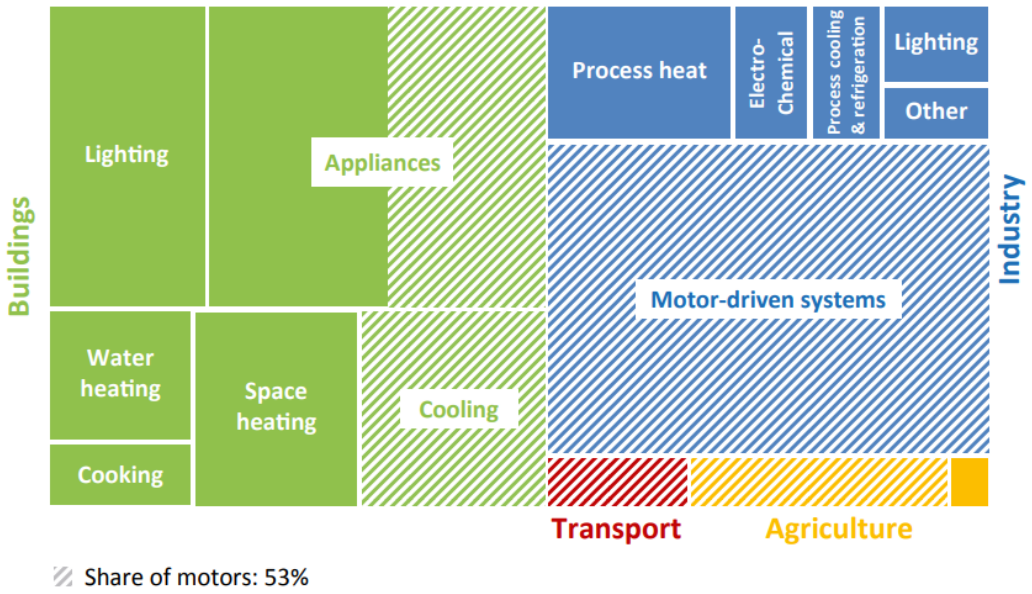

Figure 1.1: 2014 total global electricity consumption by end-use [1].

The efficiency of a motor-driven system is the product of the efficiencies of its individual components, including that of the electric motor which is currently fairly high [1]. Therefore, attention should also be given to other components in the overall system, including the end-use device such as a pump, and operator behavior like optimizing maintenance and motor selection [1]. Another opportunity to save electricity is by installing a variable frequency drive (VFD), which controls the speed of the motor to meet the energy demand during industrial processing without the need for a throttle [1]. This has the potential to improve the efficiency of variable load motor systems by 15-35% [1]. Policy-makers around the world have shifted their focus towards energy savings in the motor, end-use device, and VFD collectively. This is more important than ever as the fast adoption of electric motors is driving electricity

demand growth, estimated to double from 10500 TWh in 2014 to around 20000 TWh in 2040 [1].

The cost of saving energy is generally lower than that for increasing electricity generation (amplified by higher transmission losses) [1]. Thus, improving the efficiency of electric systems is a an attractive strategy, especially as electricity prices increase [1]. It also stimulates economic growth through competition, let alone the mitigation of climate change [1]. To limit the average global temperature increase to 2 °C by 2100, it is estimated that the average global efficiency of electric motor systems should increase by 41% in 2040 relative to 2016 [1]. Higher efficiency also leads to smaller, lighter, cheaper, and more reliable systems as they experience less thermal stress and cooling requirements become simpler. With many countries enforcing mandatory MEPS, premium efficiency motors (classified as "IE3" by the *International Electrotechnical Commission*) and above are expected to dominate in 2040 with the advent of new technology trends [13]. Announced policies suggest a cumulative investment of $350 billion into industrial motor systems from 2016 to 2040, with an average payback period of around four years at most from VFDs alone [1].

1.2 Current Technology Landscape

An emerging electric motor technology is the axial-flux permanent magnet synchronous motor (AFPMSM) with printed circuit board (PCB) stator, which offers efficiency, power density, and manufacturing cost benefits over traditional radial-flux synchronous motors [14]. They achieve speed control using VFDs to track energy demands, showing significant potential for industrial applications like pumps and fans. Unfortunately, the challenge with deploying these motors is their very low stator inductance, which is on the order of 10s of µH [15]. So, if traditional silicon (Si) based insulated-gate bipolar transistor (IGBT) devices are used in the VFD, their low maximum switching frequency of around 20 kHz would call for bulky filter components to be installed between the VFD and the motor to meet current ripple requirements, making it difficult to physically integrate the two [16, 17].

To decrease the size, weight, and cost of this system, power devices that support vastly higher switching frequencies (100s of kHz) may be used [17]. Developments in wide band gap (WBG) materials like silicon carbide (SiC) and gallium nitride (GaN) offer this benefit alongside over 50% reduced losses (switching and conduction) [17, 18]. Using WBG devices in VFDs has the potential to save around 17 TWh per

year in Europe alone [13]. As such, there are significant efforts towards the adoption of WBG semiconductors in electric drives for many applications, including petroleum refining, deep earth drilling, and electric vehicles [5, 19–21]. Many industrial motors are now embracing SiC, including *Celestica*'s PCB-stator AFPMSM (which is the electric drive that has motivated this thesis) [17]. On the other hand, GaN switches are well-known to operate more efficiently than SiC and at higher frequencies due to their lower on-state resistance, zero reverse recovery loss, and lower capacitances [17, 22, 23]. However, GaN is mostly rated for lower voltage applications, making them more suitable for consumer electronics [5, 22, 24].

Generally, most VFDs consist of an AC-DC rectification stage followed by a three-phase DC-AC voltage source inverter (VSI) [17]. In this topology, the output voltage is pulse width modulated (PWM). To achieve closed-loop position-sensorless PMSM control with model-based estimation, the output voltage of the VFD needs to be applied directly to the motor terminals [25]. This causes the VSI topology to amplify harmonics and losses in the motor as it induces large changes in flux linkage [26]. On the other hand, current source inverter (CSI) drives do mitigate motor losses via their filter capacitors [26], but have always been more expensive, inefficient, and complex to gate as they required twice the number of switches [4, 27, 28].

1.3 Research Gap and Objectives

Monolithic bidirectional (BD) high-voltage GaN is a promising technology currently being introduced to market, showing potential to leverage the benefits of GaN (improved VFD efficiency) and the CSI topology (improved motor efficiency) [6, 29]. Thus, there is an opportunity to design a CSI PMSM drive with these switches, hypothesizing cost effective and noticeable inverter and machine loss reduction. This undergraduate thesis investigates the design process and validation of a three-phase CSI prototype using research samples of *Infineon*'s brand new 650 V 14 A BD-GaN device: IGLT65R055B2 [6]. This investigation will pave the way to drive *Celestica*'s PCB-stator AFPMSM. Previous works have investigated GaN-based CSI drives [7, 28], but none have characterized machine losses of PCB-stator AFPMSMs driven by BD-GaN CSIs and compared them to those driven by SiC VSIs for evaluation.

The first objective is to design the CSI and lay out and fabricate the PCB. CSI architectures, models, and design guidelines will be used to select components and predict the operation and losses, confirmed with control-level simulations in *PLECS*

[4, 27, 30–34]. There are several CSI modulation techniques that trade off efficiency, implementation effort, and other parameters [7, 35–39]. Optimizing the modulation strategy for this project is out of scope, so, the BD-GaN switches will be gated through isolated gate drivers using space vector pulse width modulation (SVPWM), which is very popular [32, 36, 37, 40, 41]. The control will be implemented in *PLECS* for the *Texas Instruments* C2000 microcontroller [42]. The CSI will be driven by a synchronous buck converter and DC link inductor capable of outputting up to 10A [43–46]. Since gating GaN devices is sensitive to noise and ringing, there is a need to investigate PCB layout optimization for electromagnetic compatibility at high switching speeds [22, 47, 48].

The second objective is to experimentally validate the operation of the prototype board on a three-phase Wye-connected resistive load. To de-risk the testing, the board will be powered from a ≤ 30 V, 1 A input. The CSI modulation will be verified first by bypassing the buck converter and feeding the power supply in constant current mode to the switch node. Following this, DC link current regulation via the buck converter will be confirmed.

These two objectives are the first steps in paving the way for future investigation into the influence of the CSI topology on the machine losses of *Celestica*'s PCB-stator AFPMSM. These losses can be compared to those driven from a VSI topology (using the motor's built in SiC VSI) at the same output phase current amplitude (I_{out}) and switching frequency (f_s)). Overall, this thesis aims to highlight the design process for these emerging BD switches in a CSI topology, with the hopes of enabling future research efforts to set expectations for efficiency gains when transitioning VFDs for PCB-stator AFPMSMs from VSIs to BD-GaN CSIs.

Chapter 2

Background and Literature Review

2.1 Synchronous Motors

Electric machines based on the Lorentz force can operate as motors (converting electrical to mechanical power) or generators (vice versa). PMSMs are a popular type of AC electric machine for many applications, including aircraft, electric vehicles, and industry, for their fault tolerance, high efficiency, low torque ripple, and robust control [49–52]. Like all machines, they consist of a rotor (here, made from permanent magnets (PM)) and a stator. Traditionally, the stator features copper wires wound around iron cores (stator windings). In motoring operation, the stator windings are supplied with AC currents to produce a rotating magnetic field that interacts with the PMs' flux, producing a torque in the direction of rotation that tends to align the two magnetic fields [2]. Therefore, in steady-state, the rotor and its magnetic field rotate at the same angular speed (n [RPM]) as the stator's rotating magnetic field, which is proportional to the AC frequency of the stator currents (f_e [Hz]) [2].

$$n = \frac{60 f_e}{\text{poles}/2} \tag{2.1}$$

Lorentz-based machines obey electromechanical energy conservation (no energy is stored). So, as a torque is produced (proportional to the stator current), a speed voltage proportional to the angular speed is induced in the stator windings by the rotating PMs [2]. Parasitic elements include the stator windings' resistance and inductance, allowing us to model the synchronous motor using an equivalent circuit:

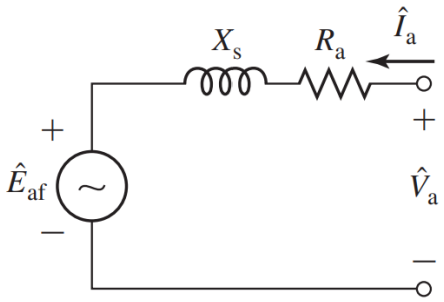

Figure 2.1: Circuit model of a synchronous motor [2].

Since most power systems are three-phase (f_e = 50 Hz or 60 Hz), synchronous machines are usually three-phase as well, where each phase is shifted by 120° from the others. Thus, an integer multiple of three coils (six coil groups, two per phase) per pole pair are required, where coils in the same phase are connected in series or parallel [2]. Traditionally, these coils are laid out around the stator to produce a radial flux according to its air gap path. Hence, these motors are called radial-flux PMSMs.

On the other hand, axial-flux configurations of PMSMs offer higher torque density and are being adopted into the same applications [53–58]. Although the stator fields can still be produced with copper wires and laminated ferromagnetic cores, there are efforts to do so with coreless PCB traces in so-called PCB-stator AFPMSMs to reduce material and process costs, size, weight, losses, and manufacturing time [14, 59–63]. Different coil patterns and geometry optimizations are being investigated, and specific tools to design PCB-stators (namely from *ECM PCB Stator Tech*) are being introduced as this technology increases in popularity [64–66]. *ECM* is partnering with several industry players, including *Celestica*, to deliver PCB-stator motors [67, 68]. Also, *Infinitum Electric* secured $185 million in funding to accelerate industrial decarbonization with their PCB-stator motors [69].

The behavior of ferromagnetic materials like iron is usually represented with B-H hysteresis loops. As the material is exposed to a magnetic field (H), which can be produced by an external current, magnetic domains in the material align with H, thus increasing the magnetic flux density (B). Removing H may still allow the material to experience B as some magnetic domains are still aligned, hence exhibiting memory (hysteresis). An iron core subject to an alternating current traverses this hysteresis loop, putting energy into and extracting some of it back from the material's magnetic dipoles [2]. The lost energy (ΔW), represented as the enclosed area of the B-H loop,

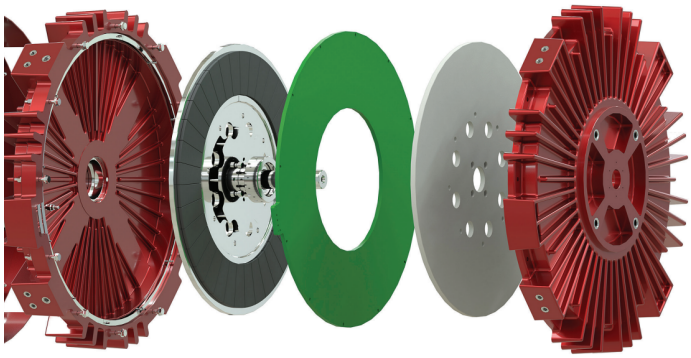

Figure 2.2: Exploded view of *Infinitum Electric*'s PCB-stator motor, showing the back motor housing, back rotor, PCB stator, front rotor, and front housing (left to right) [3].

is dissipated as heat [2].

$$P_{\text{hysteresis}} = \Delta W f_e \tag{2.2}$$

The other loss mechanism is due to eddy currents in the ferromagnetic material. From Faraday's law, a time-varying magnetic flux induces a voltage inside the core that acts as a short-circuited winding with resistivity (ρ) [2]. Induced currents circulating through the material's electrical resistance wastes power as heat. For AC stator currents producing AC flux (Φ),

$$P_{\text{eddy}} \propto \frac{\Phi_{\text{peak}} f_e^2}{\rho} \tag{2.3}$$

This is usually mitigated by laminating the core with thin sheets of the ferromagnetic material that are electrically insulated from each other [2].

In traditional core-based motors, up to a third of motor losses are due to eddy currents in the laminated core [59]. Eddy losses are more significant than hysteresis losses since they are proportional to f_e^2 rather than just f_e. Thus, coreless PCB-stator PMSMs significantly reduce losses due to the lack of iron cores [3, 14, 59, 63]. Also, without a core, as the rotor spins, its PMs experience a constant reluctance and magnetic field, mitigating their losses and hence, allowing them to be unlaminated to reduce cost [3, 59].

However, the motor often consists of other metallic parts subject to eddy loss. The PCB-stator is held in place using a supporting disk often made from stainless steel, but this can be resolved by replacing it with a nylon disk [14, 61]. The metallic motor housing, which is near the PCB-stator due to the motor's high volume density,

can experience eddy currents. If it's magnetic, it would be subject to hysteresis loss as well. Also, the stator windings experience eddy currents as the rotor spins, which is the primary source of loss in PCB-stator AFPMSMs, especially in double rotor machines like in Figure 2.2 [15, 60, 62, 63, 70]. There are harmonics in the air-gap flux density, so each harmonic component contributes to this eddy loss [60, 62]. Moreover, in effort to improve torque density, slotted magnetic cores which fit into the PCB-stator are proposed, reintroducing hysteresis core losses [71, 72]. Finally, a challenge with coreless PCB-stator AFPMSMs is their low stator inductance, which causes large torque and current ripple [15, 60]. Connecting a series inductor mitigates this but adds weight, volume, cost, and losses [60]. Another approach would be to increase the switching frequency of the motor's VFD, which is feasible with WBG switches [15, 60].

2.2 Drive Inverters

As mentioned, PMSMs are controlled by VFDs to rotate the stator magnetic field at a particular frequency. The most common VFD topology is based on the VSI [17]. Three-phase power is supplied to the input, usually from the electrical grid at 240 Vrms or 480 Vrms for industrial systems. This is followed by a three-phase rectifier parallel to a DC link capacitor that stabilizes a DC voltage (V_{dc}) (hence the term "voltage source") before it is inverted by the VSI at the desired amplitude and frequency. A three-phase VSI consists of three half-bridges (legs), where each one is composed of two switches in series and the switch node produces one of the output phases [73]. To supply an inductive load like a motor, the VSI must be able to operate in all four quadrants of the current-voltage plane, thus, the switches are typically implemented as MOSFETs or IGBT/diode pairs, which cannot reverse block [73].

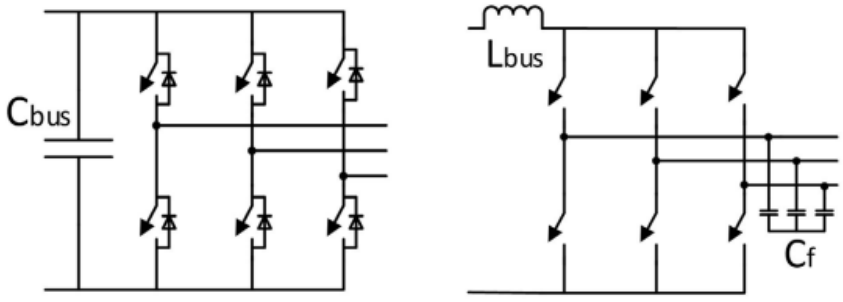

Figure 2.3: Basic topologies of a three-phase VSI (left) and CSI (right) [4].

For AC outputs, a simple gating scheme is sinusoidal PWM (SPWM). Here, a slowly-varying (fundamental frequency, f_e) sinusoidal control signal is compared to a high-frequency (switching frequency, f_s) triangular waveform, producing a time-varying duty ratio [73]. For a three-phase inverter, three control signals with amplitude V_{control}, each 120° phase-shifted from each other, are compared to the same triangular signal with amplitude V_{tri}. The amplitude modulation ratio is defined as

$$m_a = \frac{V_{\text{control}}}{V_{\text{tri}}} \tag{2.4}$$

where typically $m_a \leq 1$. The frequency modulation ratio is defined as

$$m_f = \frac{f_s}{f_e} \tag{2.5}$$

The line-to-line output voltage varies from $-V_{dc}$ to 0 to $+V_{dc}$ [73]. So, harmonics around multiples of m_f exist and the amplitude of the fundamental line-to-line rms voltage component is $\frac{\sqrt{3}}{2\sqrt{2}} m_a V_{dc}$ [73]. To avoid shorting the DC link voltage and damaging the switches, both switches in a single leg must not be gated on simultaneously. This is achieved by adding a dead time between complementary switching events [73]. SVPWM operates on a similar approach, but using space vectors to improve total harmonic distortion, bus utilization, and switching loss, at the cost of implementation complexity [74–76].

In various applications, high-precision position (angle) measurement of the rotor is critical to ensure alignment with the stator (field-oriented control) and calculate angular speed. However, position sensors are expensive and large [77]. Thus, system cost can be reduced and VFD reliability can be enhanced by employing position-sensorless control (self-sensing) [78, 79]. The most popular techniques require the VFD's output voltage to be directly applied at the motor terminals, without a filter in between to avoid resonance [25, 78]. Therefore, since the stator inductance experiences harmonic components of the PWM voltage, there may be a noticeable current ripple depending on f_s. So, VSIs can increase losses in PCB-stator AFPMSMs with magnetic housings or magnetic slotted cores [26, 80–82]. Ferromagnetic materials cycle through minor loops over f_s in their hysteresis curve when subject to PWM harmonics, increasing the total energy lost per cycle over f_e [83–86]. This high $\frac{dv}{dt}$ transience can also damage the motor insulation and reduce the motor's reliability and lifetime [26, 87].

On the other hand, CSIs are the dual to VSIs: the input appears as a DC current source stabilized by a DC link inductor [73]. They can be gated with PWM schemes similar to VSIs, including SPWM and SVPWM [32, 36–41], but require an output capacitive filter to absorb the high-frequency harmonics and prevent output voltage spikes [26, 87]. While VSIs provide open-circuit protection, CSIs offer short-circuit protection [73, 87]. Instead of a dead time, CSIs have a live time to avoid overvoltage from interrupting the DC link current [27]. Also, to avoid interphase short circuits between the output filter capacitors, the switches need to reverse block [27]. Historically, these have been implemented with thyristors for slow dynamic systems [27]. CSIs adopting MOSFETs or IGBTs for fast-switching applications need a diode in series with every switch, which increases conduction losses and cost [27]. A more efficient alternative is to have back-to-back (source- or drain-connected) unidirectional switches and leveraging their body diodes, but this complicates the gating scheme without reducing cost [27].

Since DC current sources are not available, several pre-stage topologies exist to control the DC link current (I_{dc}), including the buck converter [27, 43–46]. The full-bridge enables regeneration but requires double the switches, hence doubling the cost, losses, and complexity [27]. Since industrial applications usually only focus on motoring (no regeneration), the buck converter will be adopted as this also de-risks the project. The amplitude modulation ratio (m_a) is designed to be around 1 to minimize conduction losses as the DC link current does not have to be greater than the desired fundamental phase current magnitude (I_{out}) [27].

$$I_{out} = m_a I_{dc} \tag{2.6}$$

The DC link inductor and output filter capacitors are sized using the following:

$$L_{dc} = \frac{\sqrt{3} V_{ln}}{4 f_s \Delta i_{Ldc-pp}} \tag{2.7}$$

$$C_f = \frac{I_{dc}}{4 f_s \Delta v_{Cf-pp}} \tag{2.8}$$

where V_{ln} is the phase-to-neutral voltage, Δi_{Ldc-pp} is the peak-to-peak DC link inductor current ripple (usually 10% of the rated phase current), I_{dc} is the DC link current, and Δv_{Cf-pp} is the peak-to-peak output filter capacitor voltage ripple (usually 5% of the rated line-to-line voltage) [4, 30]. These equations assume an ideal DC link current, so f_s refers to the CSI switching frequency. Introducing another switching

frequency from the buck complicates the design equation, but (2.7) and (2.8) will still be used as approximations (where f_s still refers to the CSI switching frequency).

The mandatory output capacitive filter defines a smooth sinusoidal output voltage, lowering $\frac{dv}{dt}$ and improving motor loss performance over VSIs as harmonic components are attenuated [26, 30, 87]. Also, CSIs have less electromagnetic interference (EMI) and are more fault tolerant than VSIs [17]. Coupled with the ability to perform position-sensorless control among other benefits [88], CSIs are regaining popularity [4, 27, 89–91]. This is especially the case with the advent of efficient WBG devices, which is discussed in Section 2.4.

2.3 Gallium Nitride Devices

WBG semiconductor devices are being widely adopted for high-speed, high-efficiency power conversion, embraced to replace Si-based devices [22]. Among them, GaN high electron mobility transistors (HEMT) offer very low on-state resistances (R_{on}, with a positive temperature coefficient) due to the formation of a high mobility 2D electron gas [22]. Thus, for a given current rating, GaN HEMTs can achieve a die size smaller than Si switches, leading to lower parasitic capacitances, faster switching speeds, and lower switching loss [22]. From (2.7), higher switching frequencies afforded by the low capacitances can reduce the CSI DC link inductor's size, weight, and cost. Moreover, GaN HEMTs can reverse conduct, but unlike Si and SiC devices, they do not exhibit a parasitic body diode, so there are no reverse recovery losses [92].

However, key challenges with GaN include high $\frac{di}{dt}$ which produces EMI and parasitic inductance voltage spikes and ringing [22]. High $\frac{dv}{dt}$ leads to displacement currents in parasitic capacitances that pull up the gate voltage, which can mistrigger the switch because of its low threshold voltage ($V_{th} \approx 1$ V) [22]. A common solution is to turn it off at a negative gate voltage, which also decreases switching-off loss, but at the cost of elevated reverse conduction loss [93]. The fragile Schottky gate is susceptible to overvoltage, lowering the gate voltage margin and thus making it susceptible to noise [22]. Furthermore, like any transistor, Miller plateau during gating transients increases switching loss [94]. This can be minimized by driving the gate with a larger current, but at the expense of EMI as mentioned [94]. A Kelvin source connection improves noise immunity by minimizing the gate loop inductance while decoupling it from the power loop [95].

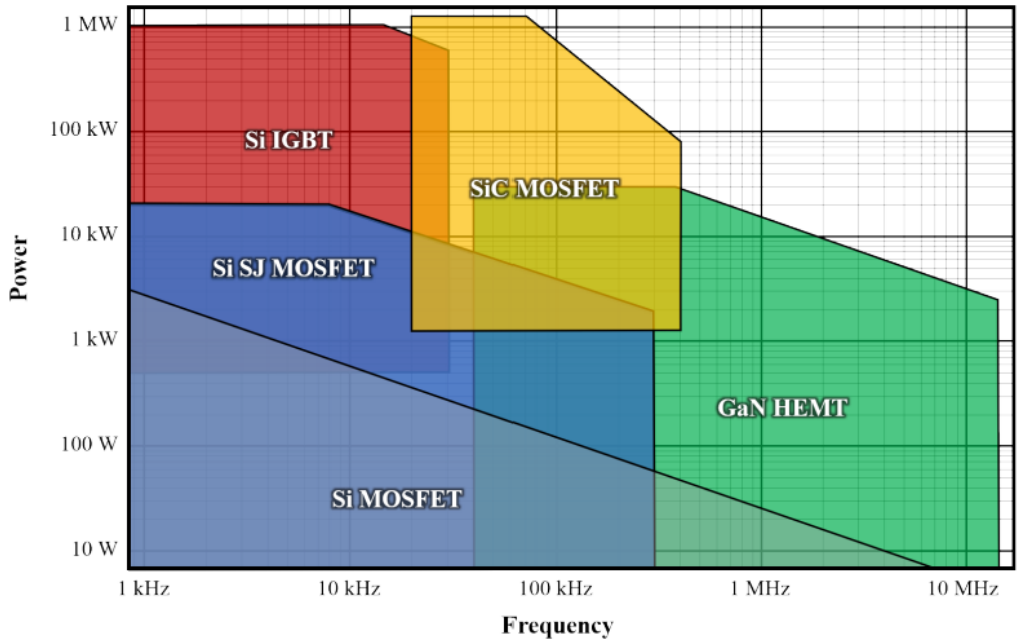

Figure 2.4: Frequency and power regions for different power semiconductor technologies [5].

There are several players offering GaN power HEMTs and solutions, including *EPC*, *Texas Instruments*, *Infineon* (*GaN Systems*), *Nexperia*, *Transphorm*, and *IGaN-Power* [22]. However, unlike IGBTs and SiC MOSFETs, which can have kV ratings, most GaN devices have a breakdown voltage of 650 V as they are lateral devices [5]. *Transphorm* and *IGaNPower* have 900 V offerings, and the latter is the first to offer 1200 V [5]. Enhancement mode (normally-off, $V_{th} > 0$) devices are usually more desirable to work with than depletion mode (normally-on, $V_{th} < 0$) ones to minimize the risk of shoot-through [22]. To use depletion mode devices as normally-off, cascode and direct drive topologies can be implemented by adding a series Si MOSFET [22]. This improves the robustness by increasing V_{th} but at the cost of increased conduction, switching, and reverse recovery losses.

There are several research areas with GaN, including vertical drift epitaxy to increase the breakdown voltage (which would be useful for high voltage applications such as VFDs being supplied from 480 Vrms grids) [96], monolithically-integrated gate drivers [97], and monolithic bidirectional (BD) devices. The latter is the most promising for CSIs as they can reduce component count, cost, and losses. They may even popularize AC-AC converters like matrix converters, bypassing the DC link and increasing power density at very low cost [98]. *Panasonic* has studied BD-GaN switches, but have never made them publicly available [7, 98–100]. *Nexperia*

and *Infineon* are catching up to this technology and commercializing them [6, 29]. *Infineon* is offering research samples of their 40V (single-gate) and 650V (dual-gate) *CoolGaN BDS* enhancement mode switches, with plans of releasing an 850V device later this year [6]. These high voltage offerings call for adoption in higher power applications.

With the help of *Celestica*, we received samples of *Infineon*'s 650V 14A devices (IGLT65R055B2) and had the chance to meet with *Infineon*'s application engineer twice (on October 25, 2024 and December 11, 2024) to learn about these devices and best practices. Rather than having two source- or drain- connected switches which would double R_{on}, this BD device has two gates and two sources, using the same channel at around 1.15 times the length of a unidirectional device. Thus, R_{on} only increases by 15% and saves die area. Rather than a Schottky gate contact, an Ohmic gate contact is used (gate injection transistor), so the gate should be driven by a current source (usually implemented as a voltage source and resistor in series, realizable with traditional gate drivers).

For fast turn-on and turn-off, a speed-up capacitor circuit is recommended to transiently inject or remove charge quickly. Since the gate voltage changes with source current, using a voltage source plus resistor instead of a current source for gating requires careful selection of the voltage and resistance to restrict the gate current variation. As with the unidirectional devices, these BD switches have a low V_{th}, so a negative turn-off bias as well as a low-impedance turn-off path (compact layout plus low $R_{\mathrm{g-off}}$) that shunts the displacement current away from the Ohmic gate contact are required.

Two gates requires two gate drivers, each referenced with respect to their nearest Kelvin source. As such, there are four modes of operation according to the effective equivalent symbol in Figure 2.6: closed switch, open switch, and two diode modes in either direction. In a CSI, it can be modulated with a four-step commutation scheme to minimize conduction losses without risking interphase short-circuits [27]. However, this may add switching losses and complicates gating. Another approach is to permanently turn off one of the gates in diode mode to act as the in-series diode [27]. This approach is simpler since half the gating signals (half the cost) are needed because the gate can simply be shorted to the Kelvin source. However, this makes the turn off less stable since the gate voltage is very close to the threshold voltage. On the other hand, permanently driving the gate with a negative voltage has the same

benefit of simplified control, but although the turn-off is more stable, it increases cost and decreases efficiency due to increased reverse conduction loss (the voltage drop can be as high as 3 V) [92].

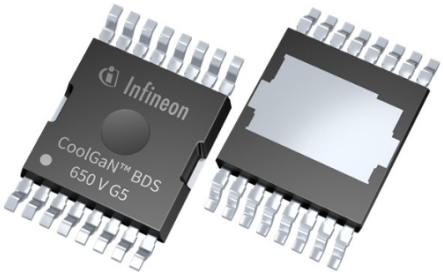

Figure 2.5: *Infineon*'s 650 V monolithic bidirectional GaN HEMT (IGLT65R055B2) [6].

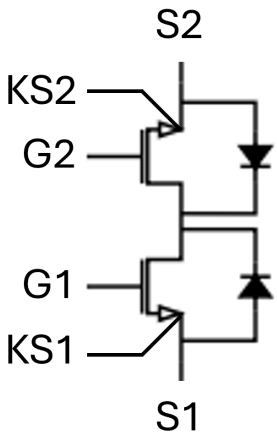

Figure 2.6: Effective equivalent circuit of the IGLT65R055B2.

2.4 Relevant Work and Gap

Infineon's BD-GaN device has not been used in a CSI yet. Regardless, many prior works have studied WBG CSIs by using back-to-back unidirectional switches instead [4, 28, 101–107]. The popularity of this research area implies significant demand and potential for these BD-GaN devices to be used in CSIs. [101, 102] predicts an improvement of up to 0.7% efficiency from SiC FET plus diode to a monolithic BD-SiC device. [28] explored driving a three-phase low-inductance load with a low-voltage GaN CSI, focusing more on layout optimization. Unlike the other papers, [7] has used research samples of *Panasonic*'s monolithic BD-GaN switches for a CSI, but has focused on optimizing the modulation scheme without experimentally characterizing motor losses.

The efficiency gains offered by enhancement mode BD-GaN devices coupled with the motor loss and reliability benefits of the CSI topology make a compelling case to design a three-phase CSI using the IGLT65R055B2 to improve the performance of PCB-stator AFPMSMs with integrated VFDs for industrial applications. Especially considering that one factor slowing down the adoption of these motors is their metallic housings heating up when driven by integrated VSIs. As mentioned, no prior works have used high-voltage, commercially-available, enhancement mode BD-GaN switches in the application of an industrial motor CSI drive, specifically for PCB-stator AFPMSMs. Nor have they compared the effects of the VSI and CSI topologies on the losses of this type of machine (at the same I_{out} and f_s). Therefore, this thesis focuses on executing the first steps towards addressing this gap in current knowledge of the field.

Chapter 3

Design Process

3.1 System Architecture

The three-phase CSI architecture features a GaN-based synchronous buck pre-stage, followed by a DC link inductor, the three CSI legs built with IGLT65R055B2 devices, and the capacitive output filter. CSI and pre-stage architectures with higher efficiency and other benefits trade off simplicity and cost, including the number of gating signals which are limited here by our digital signal processor (DSP) [27]. Here, a simpler topology is adopted to minimize points of failure, especially as this is the first project exploring these technologies. Since this is an exploration effort, cost is not a critical requirement. The CSI is designed and implemented on a PCB using *Altium Designer* with future plans to drive *Celestica*'s PCB-stator AFPMSM at $m_a = 1$ and $f_e = 60$ Hz.

At most, for four-step commutation, 14 gating signals are required (2 for the buck and 2×6 for the inverter). At least eight signals are required if the BD switches will have a gate permanently off in diode mode. As such, the DC link current control and gating is performed with a *Texas Instruments* LAUNCHXL-F28379D development platform based on the C2000 DSP as it offers 14 high-resolution (100MHz) PWM outputs and 12-bit analog to digital converters (ADC) [108]. Also, it can easily be programmed with block-based automatic code generation using the C2000 software development kit in *PLECS*, a power electronics simulation and control tool.

The thesis's theme around GaN and its efficiency encourages using unidirectional GaN HEMTs for the synchronous buck converter pre-stage. *Infineon*'s 700V 40A

GS-065-030-6-LR enhancement mode GaN HEMT is selected [109]. A rectifier stage is not included as part of the requirement around simplicity. Therefore, a DC voltage is directly supplied to the CSI input. Based on the maximum current rating of the IGLT65R055B2 devices, I_{dc} is designed for up to 10A. Based on all the switches' voltage ratings and application around industrial motor systems, the input voltage is 340 V at most (based on a 240 Vrms grid supply). The switching frequency of the pre-stage and inverter ranges from 50 kHz to 200 kHz. Therefore, using (2.7) and (2.8), $L_{dc} = 1.1$ mH and $C_f = 2.2$ μF.

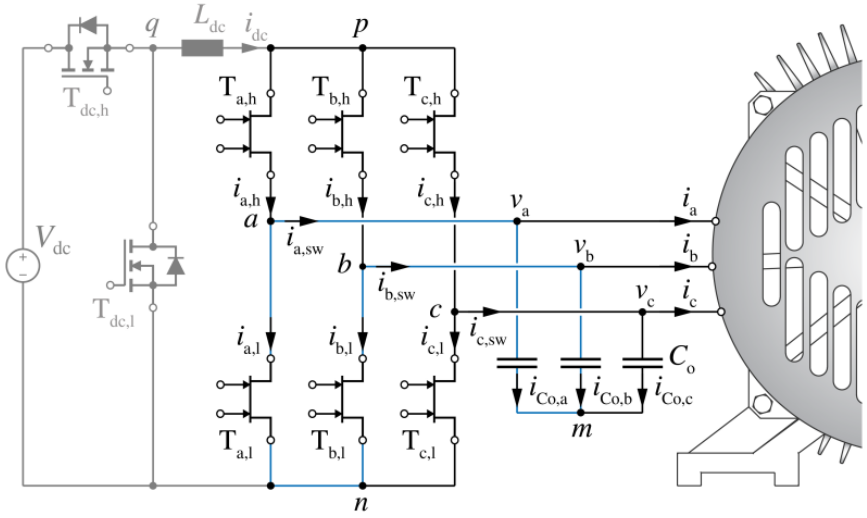

Figure 3.1: The CSI architecture to be implemented [7].

Table 3.1: Summary of key design components.

Description	Count	Part Number	Manufacturer	Comments
BD-GaN	6	IGLT65R055B2	Infineon Technologies	650V 14A
GaN HEMT	2	GS-065-030-6-LR	Infineon Technologies	700V 40A
DSP	1	LAUNCHXL-F28379D	Texas Instruments	
Buck driver	1	Si8273	Silicon Labs	
BD-GaN driver	12	1EDB8275F	Infineon Technologies	
Hall sensor	4	TMCS1123B4A	Texas Instruments	100mV/A

3.2 Circuit Design

The design process was iterative and had several design reviews, so only the current design is presented. Due to duplicate circuit elements (switches, drivers, power supplies, etc.), the PCB design is done with hierarchical schematics. As part of design-for-testing (DFT) requirements, LED indicators and test points are added to

ease troubleshooting and confirm functionality. Moreover, a design requirement is that the logic and ADC signals must be isolated from the power circuit through the use of isolated gate drivers and power supplies.

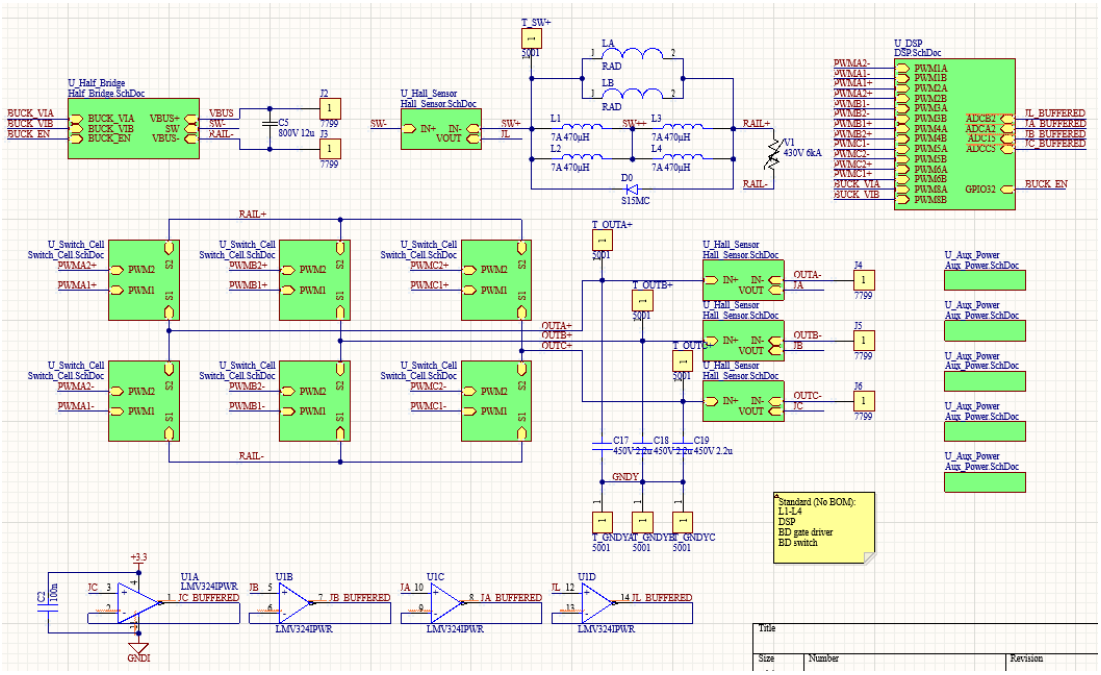

Figure 3.2: The top-level schematic.

3.2.1 Synchronous Buck Converter

The synchronous buck converter features two GS-065-030-6-LR in a half-bridge topology, with a DC link capacitor and RC snubber circuits. Due to the fast switching speeds, RC snubbers are a cheap and effective solution to protect against voltage transients, thus increasing the devices' lifespans [110]. The snubber capacitor is larger than the output capacitance of the switch to provide a low impedance path for voltage spikes and oscillations, while the snubber resistor provides damping and dissipates the power externally from the switch.

The *Silicon Labs* Si8273 half-bridge driver is selected because it is recommended by several GaN suppliers, has high common-mode transience immunity (200 kV/s, useful for high switching speeds), is isolated, supports a bus voltage up to 1500 V, and offers shoot-through protection [93, 94, 111]. This is a bootstrapped gate driver, so a high-speed Schottky bootstrap diode capable of blocking the full DC input is added alongside a bootstrap capacitor sized to balance ripple and refresh time [112, 113]. A bootstrap resistor serves to minimize the inrush current during startup. The optimum

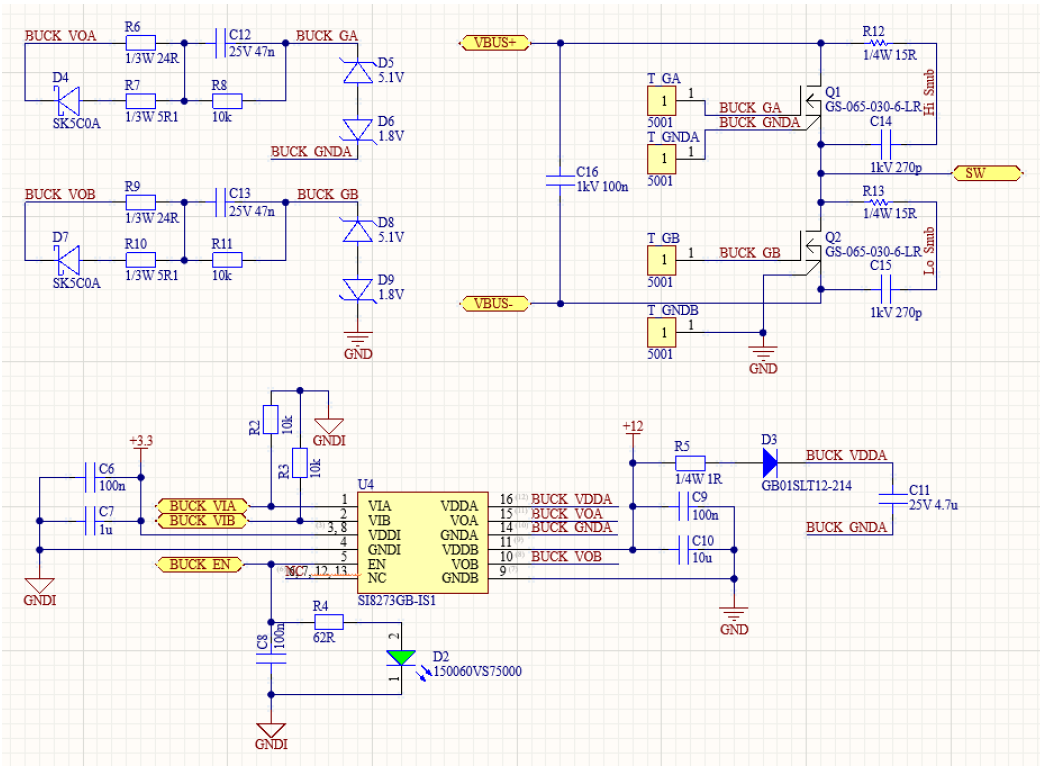

Figure 3.3: Schematic of the synchronous buck converter.

dead time depends on the DC bus voltage and switching current [93]. In this case, 50 ns is selected, which exceeds the minimum value set by the DSP's PWM resolution of 10 ns [93].

Based on reference designs and the datasheet, the turn-on and turn-off gate voltages are +6 V and −3 V respectively [93, 109]. Since the bootstrapping causes the driver to output 0 V and positive voltages, a level-shifting circuit needs to be designed and implemented [93, 95, 114]. This uses a capacitor and back-to-back anti-series Zener diodes to clamp positive and negative voltages at the gate. Stabilizing the turn-on voltage minimizes risk of gate overvoltage, and the Zener diodes create a low impedance path for displacement currents through the gate-drain capacitor, thus mitigating parasitic turn-on due to high $\frac{dv}{dt}$.

Turn-on (R_{g-on}) and turn-off (R_{g-off}) gate resistors control the rate of the gate capacitance charging and discharging respectively. Here, $R_{g-off} < R_{g-on}$ to avoid shoot-through by guaranteeing a switch turns off before the complementary one turns on. A small R_{g-off} also mitigates parasitic Miller turn-on. Increasing the gate resistance reduces EMI and ringing but at the cost of reduced switching speed and longer Miller plateau. The resistor values need to be optimized to achieve slight underdamping in

the gate voltage waveform. They are selected by referring to previous work in lab and reference designs [94, 114].

3.2.2 Bidirectional GaN

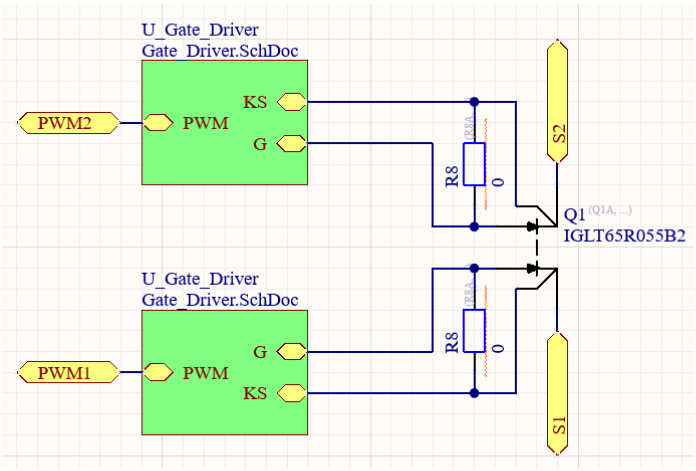

Figure 3.4: Schematic of the switch cell.

As there are effectively two sub-switches per BD-GaN switch (from Figure 2.6), two gate drivers per switch are required. However, since for a CSI, the sub-switch whose reverse conduction path is aligned with I_{dc} (the top sub-switch) can be permanently off (in diode mode) at the cost of lowered efficiency, an optional 0 Ω resistor is added to short the gate and Kelvin source of that sub-switch. Alternatively, a constant −3 V may be outputted from the gate driver, but this would increase reverse conduction loss. From our meeting with *Infineon*'s application engineer, applying 0 V via a 0 Ω resistor should not pose mistriggering risks if the layout inductance is small. However, in the case that there is not enough headroom below V_{th}, the gate driver can be used instead. The gate driver can also be employed in case four-step commutation is implemented to improve efficiency by reducing reverse conduction loss (more than it increases switching loss).

The gate driving circuit is adopted from a reference design of a Vienna rectifier that is kindly provided by *Infineon*. Based on that, the source and sink voltages should be +9 V and −3 V respectively. Therefore, a 9.1 V Zener diode and resistor are used to split the output of a 12V/12V isolated DC-DC power supply [93]. The high $\frac{dv}{dt}$ of these BD-GaN switches can induce large displacement currents through the isolation capacitance of the power supply (on the order of 10s of pF). Therefore, the ferrite beads are designed to suppress any EMI which may break the isolation

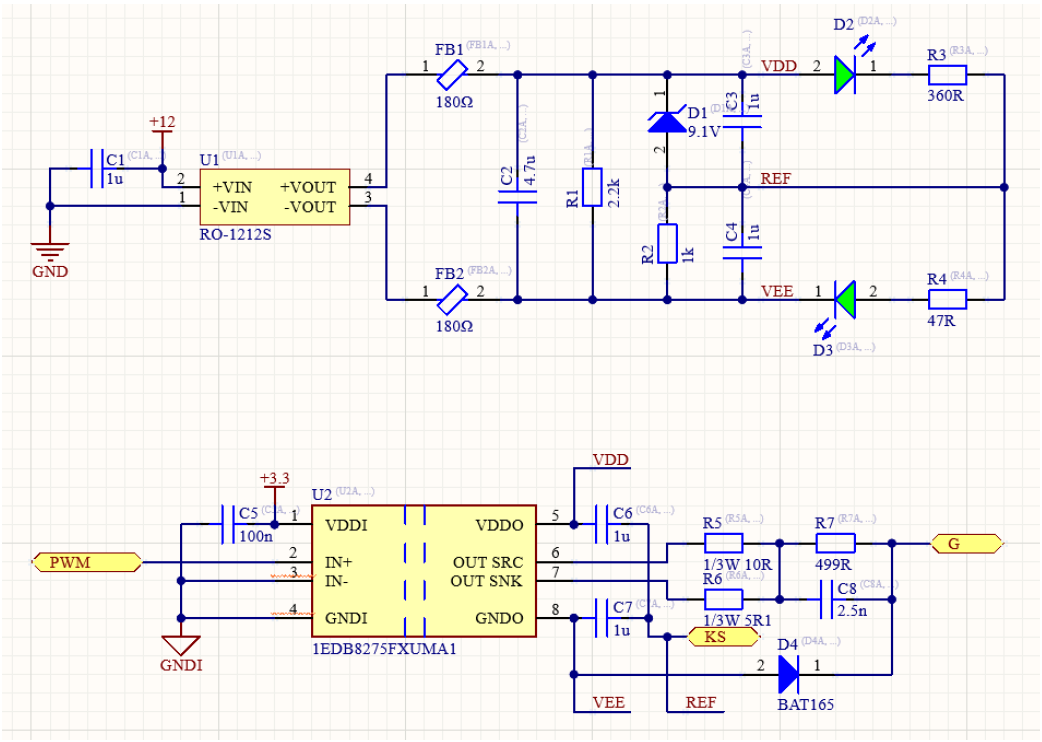

Figure 3.5: Schematic of the BD-GaN gate driver.

barrier. Otherwise, the gate resistance values need to be increased, slowing down the switch and increasing losses, which defeats the philosophy of using GaN. A custom power supply with low capacitance is another option, but this adds additional project complexity and points of failure.

3.2.3 Hall Sensor

For I_{dc} regulation and monitoring the output phase currents, the *Texas Instruments* TMCS1123B4A Hall sensor is selected for its high signal bandwidth (250kHz) and ability to measure large positive and negative currents [115]. A low-pass RC filter (filtering out the buck's switching frequency) and buffer condition the output signal before being read by the DSP's ADC. Since over-current protection is not required, the other pins are unused.

3.2.4 Miscellaneous

There are several other design features and decisions which are worth highlighting:

- Since high inductance, high current inductors are expensive, the 1.1 mH 11 A inductor is implemented as two 2.2 mH 5.7 A inductors in parallel.

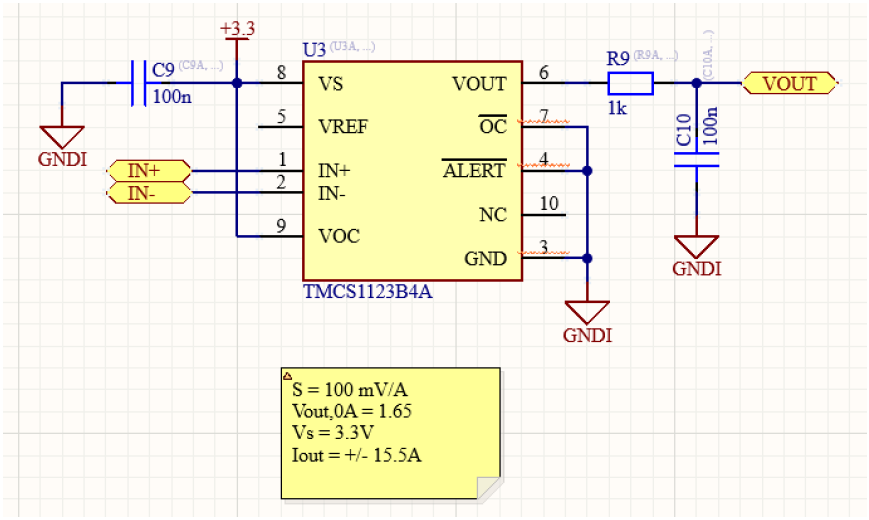

Figure 3.6: Schematic of the Hall sensor.

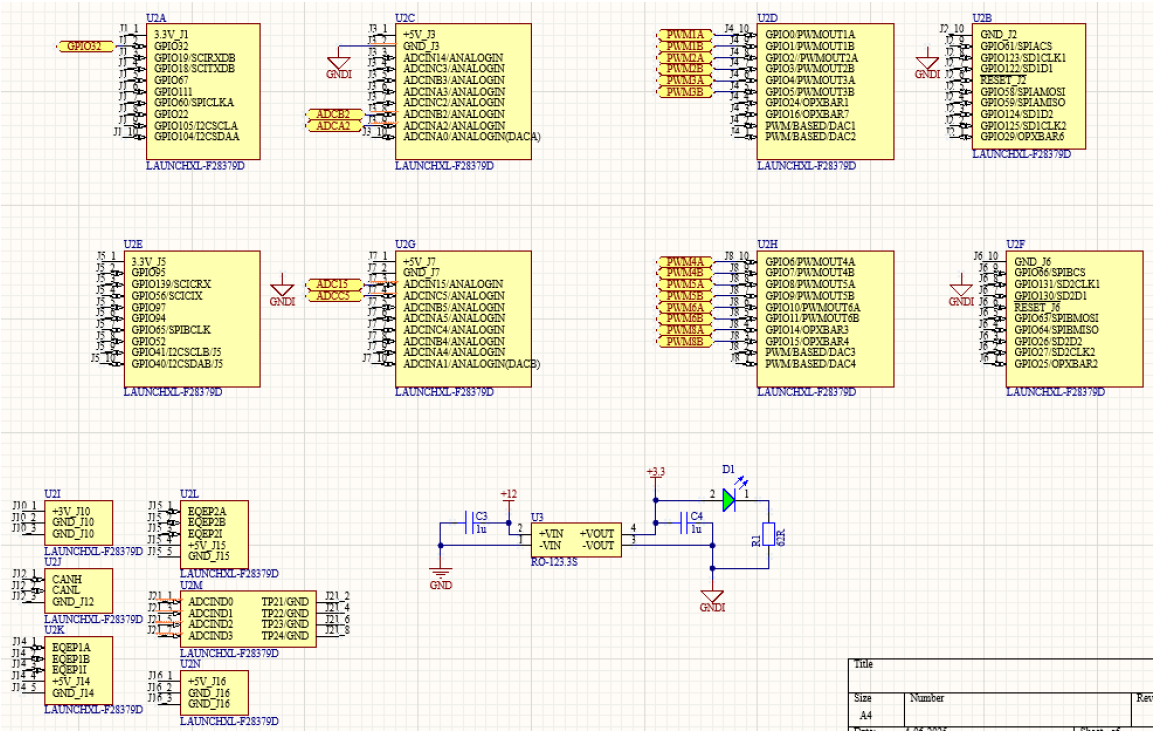

Figure 3.7: Schematic of the DSP signals and power.

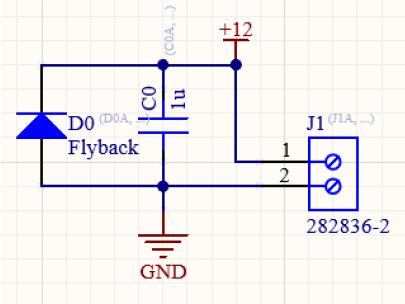

Figure 3.8: Schematic of the 12 V auxiliary supply.

- The capacitive output filter is implemented with ceramic capacitors [116].
- Since there are several integrated chips which require control-side power (gate drivers, Hall sensors), a 12V/3V3 isolated DC-DC power supply is used rather than relying on the power pins of the DSP, which would not supply enough quiescent current to all the components.
- To protect against potential I_{dc} interruptions by not implementing live time correctly, a varistor rated for 25% higher than the DC bus voltage is selected (430 V 6 kA) [117]. Since they usually fail in short circuit, no extra protection circuitry is required [117]. Note that a flyback diode is not suitable since L_{dc} will be discharged by a negative voltage from the output filter capacitor.
- Five screw terminal blocks for 12 V external power are implemented, four for the cooling fans, and one for the input supply, which drives the fans and all the isolated power supplies.
- High current (30 A) screw terminal power taps with M4 screws are used to connect to large spade connectors for robustness.

3.3 Board Layout

As part of design-for-manufacturing (DFM) requirements, most components are placed on the same layer (top) and design rules are adopted from *PCBWay*'s fabrication capabilities [118]. To simplify routing and increase power density at an affordable cost, a four layer PCB stackup is used. Up to 200 kHz switching frequency, there is no need to worry about impedance and length matching, although signal traces should be routed over their respective ground planes as much as possible.

To mitigate the effects of EMI, the signal and power paths are physically separated

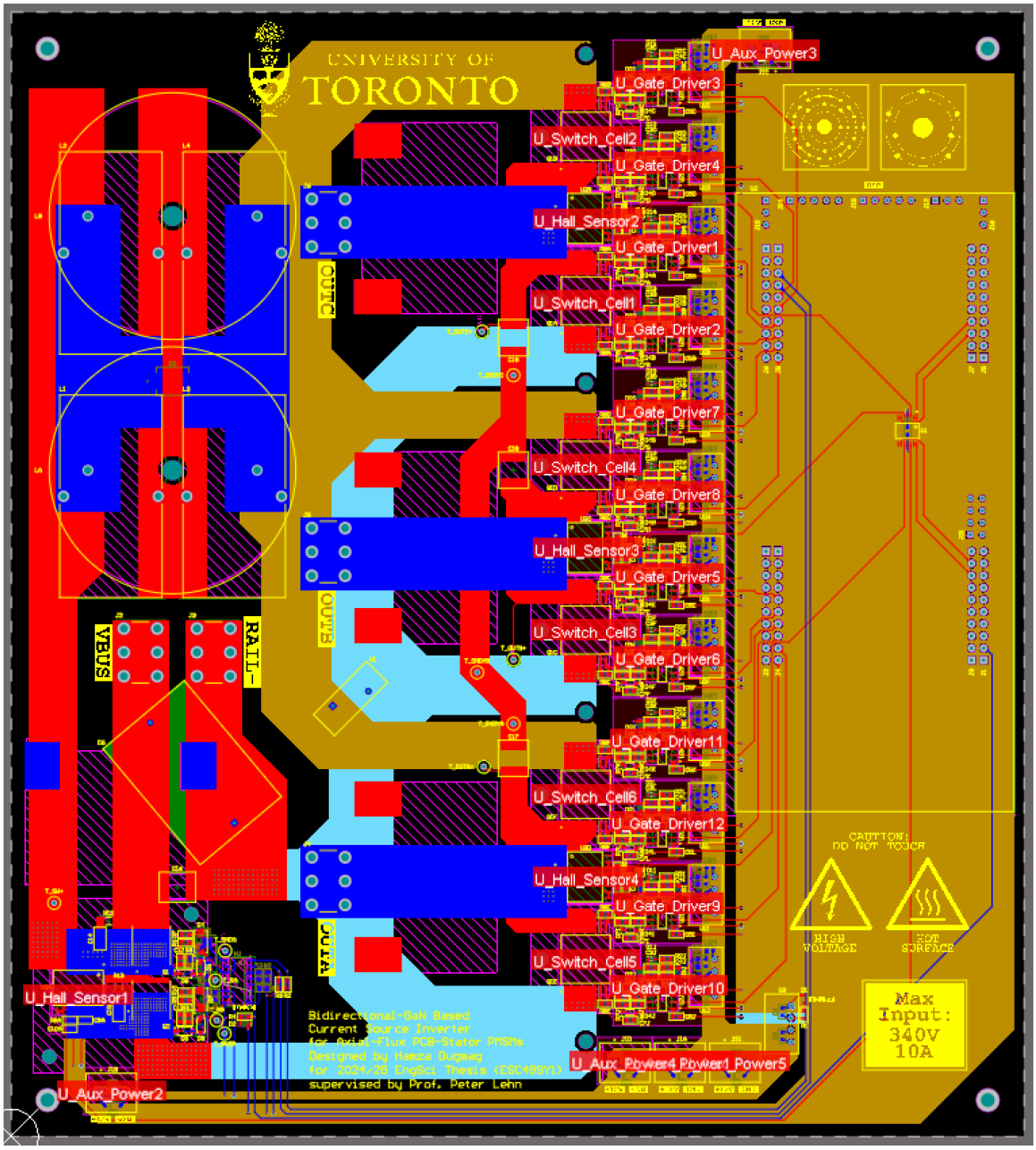

Figure 3.9: 2D layout of the entire PCB.

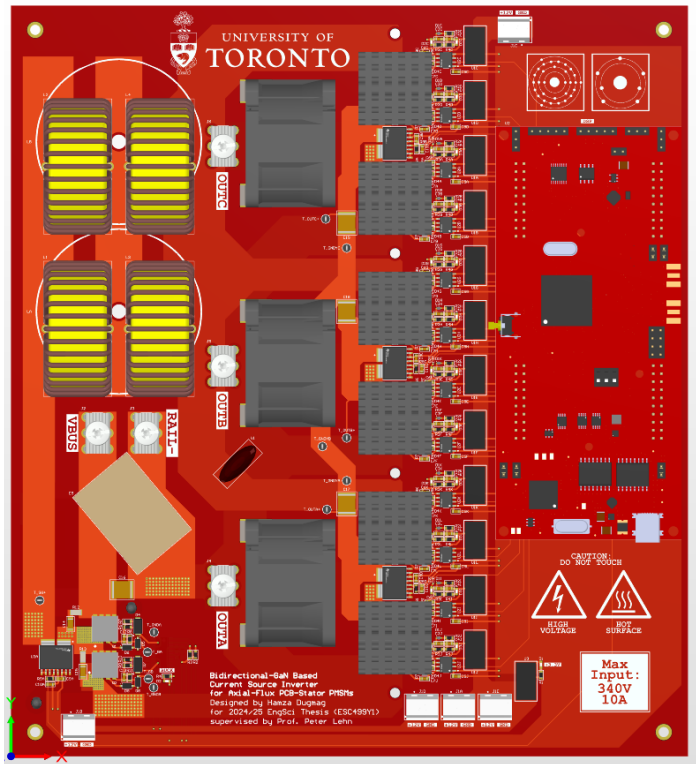

Figure 3.10: 3D orthographic layout of the entire top layer.

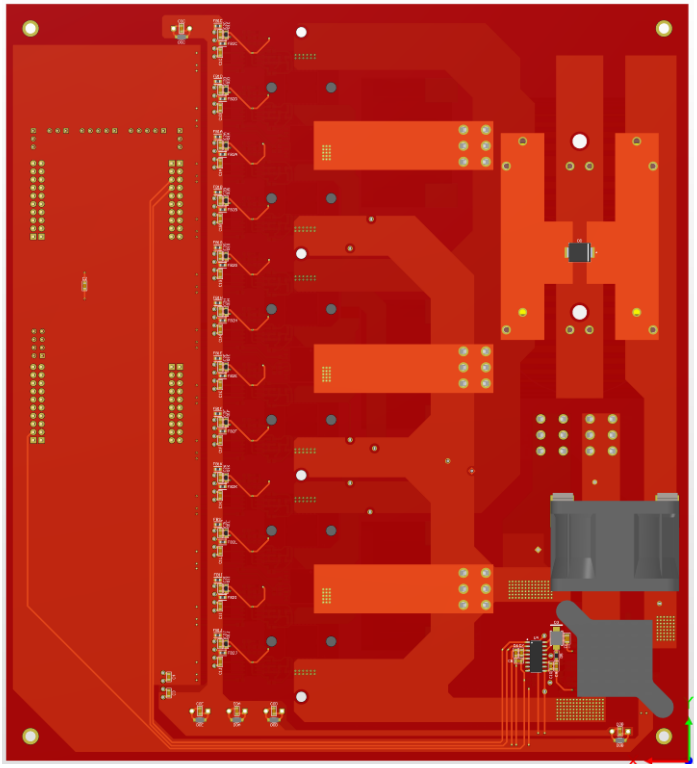

Figure 3.11: 3D orthographic layout of the entire bottom layer.

from each other to different regions on the board (i.e., the signal paths are not fully enclosed by power loops). Moreover, to avoid flashover and overheating, the power trace are sized and routed according to the IPC-2221 standard for trace width and trace clearance, where a 25% factor of safety is used [119, 120].

There is no SPICE model or relevant datasheet information of the IGLT65R055B2 to estimate switching losses. Therefore, the thermal design is based on a conservative worst-case scenario, where the switching losses equal the conduction losses [116]. Since R_{on} has a positive temperature coefficient, the maximum junction temperature is assumed (150 °C). Each switch on a leg will experience half the output phase current on average, so at $I_{ds} = 10$ A and a diode mode voltage drop of 3 V, the power dissipated by each switch is under 20 W (dominated by the diode power, which can be significantly reduced with four-step commutation or holding $V_{gs} = 0$ V). The heatsinks (black anodized aluminum to probe with a thermal camera), thermal interface material, and fans are selected accordingly. If the switches overheat, the current may be throttled. This is acceptable for this project since all that matters is validating that the CSI operates correctly. Thermal throttling will just restrict our input power range.

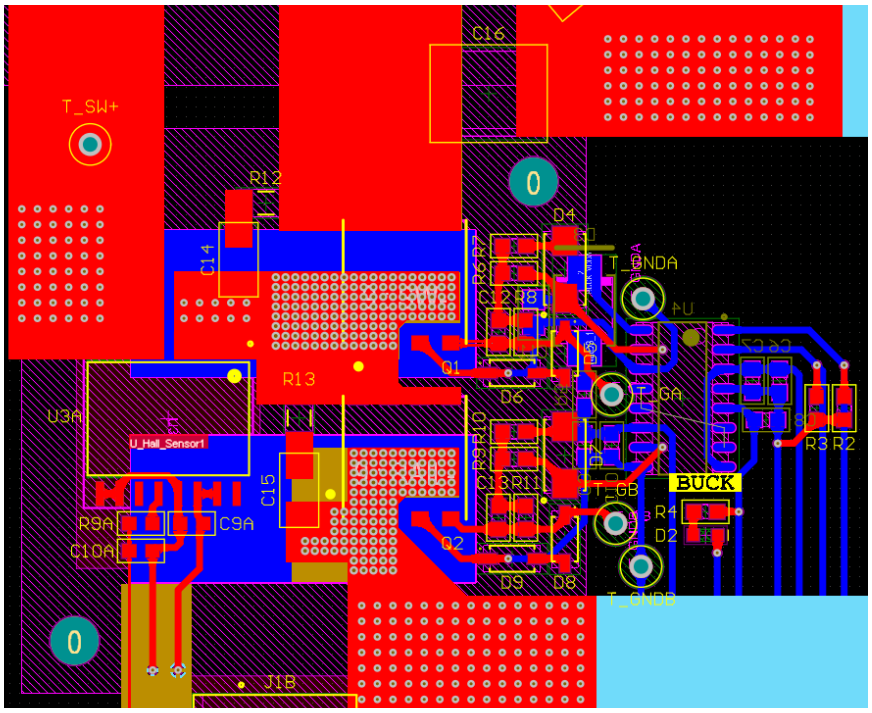

Figure 3.12: 2D layout of synchronous buck converter.

For the synchronous buck converter, the GS-065-030-6-LR devices are bottom-

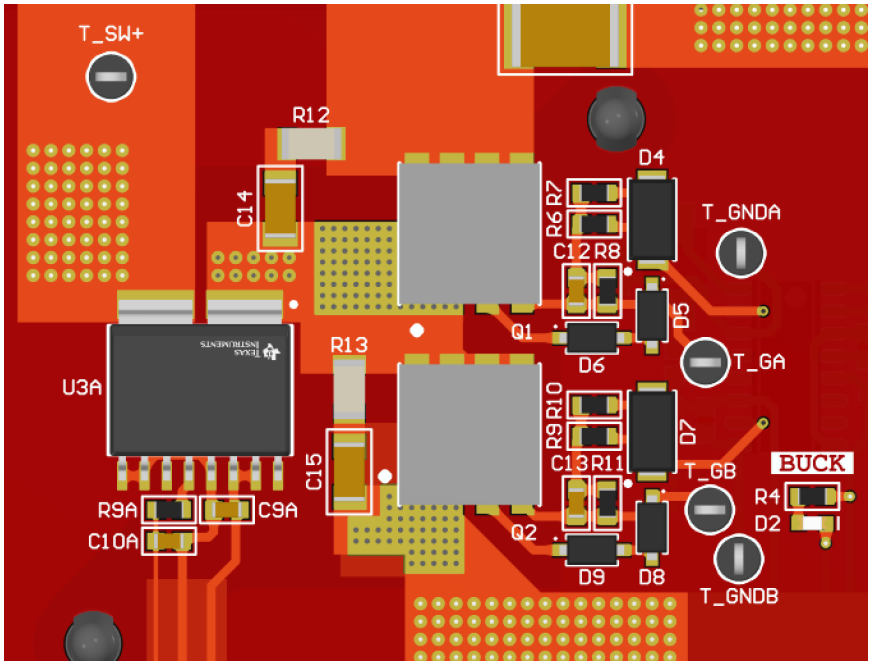

Figure 3.13: 3D orthographic layout of synchronous buck converter.

cooled, so thermal vias are required. Reference designs are used to layout the vias, with internal copper layers added to improve vertical heat transfer and horizontal heat spreading [121, 122]. Moreover, the power loop inductance must be minimized to commutate the current as fast as possible and avoid overvoltage across the switches during dead time. This is achieved by placing the DC link ceramic capacitor and both switches all near each other, while laying out the traces compactly. The layout of the Hall sensor is adopted from the component's datasheet [115].

The buck's gate driver and level-shifting components are compactly laid out on the same layer with minimal vias to minimize the gate loop inductance and turn-off path impedance. However, some the gating input signals pass over the bottom rail of the CSI, which carries I_{dc}. DC current ripple may induce current on the signal traces, which may cause mistriggering due to the high input impedance of the driver pins. This is mitigated by adding pull-down resistors at these pins. A similar layout strategy is employed for the gate drivers of the BD-GaN devices. Finally, to avoid resonance at the output filter capacitors, layout inductance is minimized there.

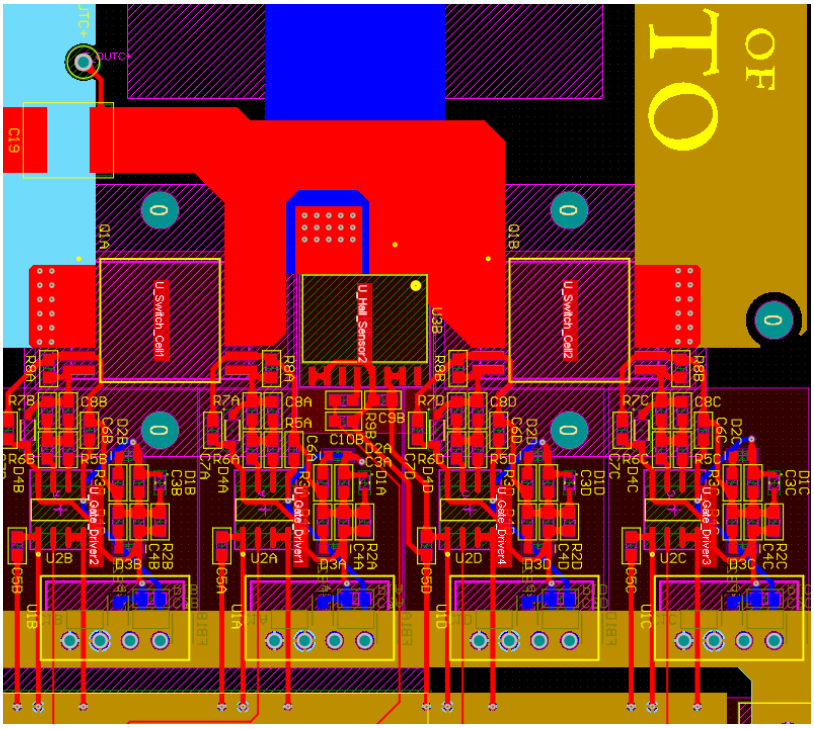

Figure 3.14: 2D layout of a CSI leg.

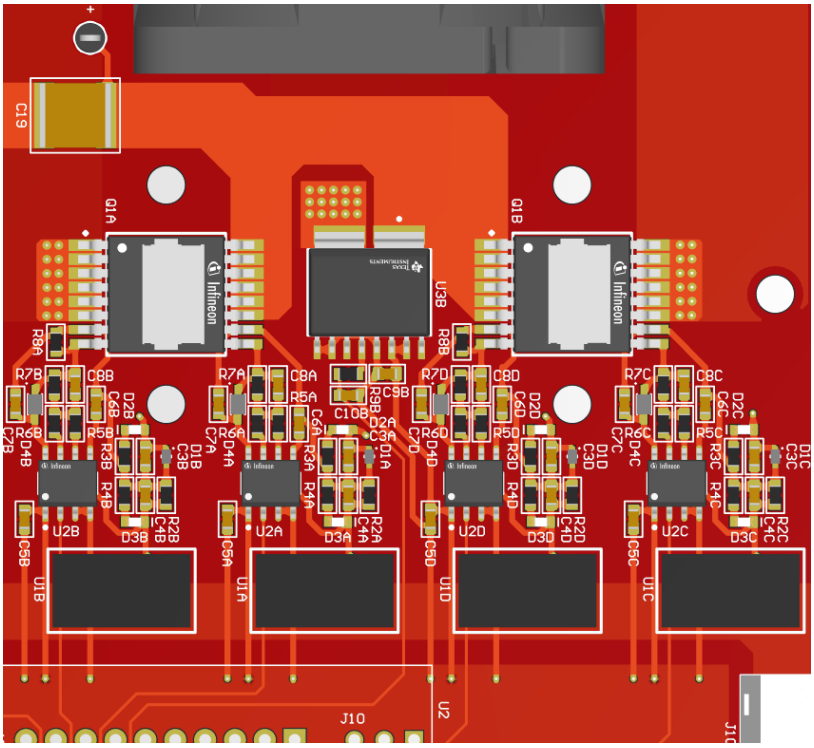

Figure 3.15: 3D orthographic layout of a CSI leg (heatsink and DSP 3D bodies removed).

3.4 Assembly

The board was fabricated through *PCBWay* with the specifications in Table 3.2. S1000H TG150 is selected as the FR4 material due to its high thermal stability, CAF resistance, mechanical strength (withstand flexing due to the heavy on-board DC link inductor) [123]. Plus, it is suitable for lead-free soldering processes, which is how it will be assembled [123].

Table 3.2: Summary of PCB fabrication specifications from *PCBWay*.

Specification	**Selection**
Layers	4 Layers
FR4-TG	S1000H TG150
Thickness	1.6mm
Minimum Track/Spacing	8/8mil
Minimum Hole Size	0.25mm
Surface Finish	1U" Immersion Gold (ENIG)
Via Process	Tenting Vias
Finished Copper	2oz
Inner Copper	1.5oz

A stencil of the top-layer is used to deposit lead-free solder paste on the component pads. After placing the surface mount components, the board is baked in a solder reflow oven. This process saves time and reduces the risk of assembly error. Finally, through-hole and bottom-layer surface mount components are hand-soldered. Visual inspection and a digital multimeter are used for continuity checks (proper connections with no solder bridges), diode polarity checks, and confirming resistor values.

Since the thermal interface material was not as adhesive as expected and the holes next to each BD switch were not spaced far enough, the only available cooling solution for these devices was to solder the heatsinks directly onto the thermal pads. Although the anodized aluminum material is electrically insulating, these heat sinks should still be considered live. Luckily, this provides the lowest resistance thermal chain.

3.5 Firmware

Current-type SVPWM control is implemented in *PLECS* for the DSP target. The firmware is adopted from a current source inverter example design provided by *Plexim* [42]. It is similar to a buck-type rectifier modulation scheme, with the only difference being that the freewheeling state is implemented using a live time (D_{live}) across the

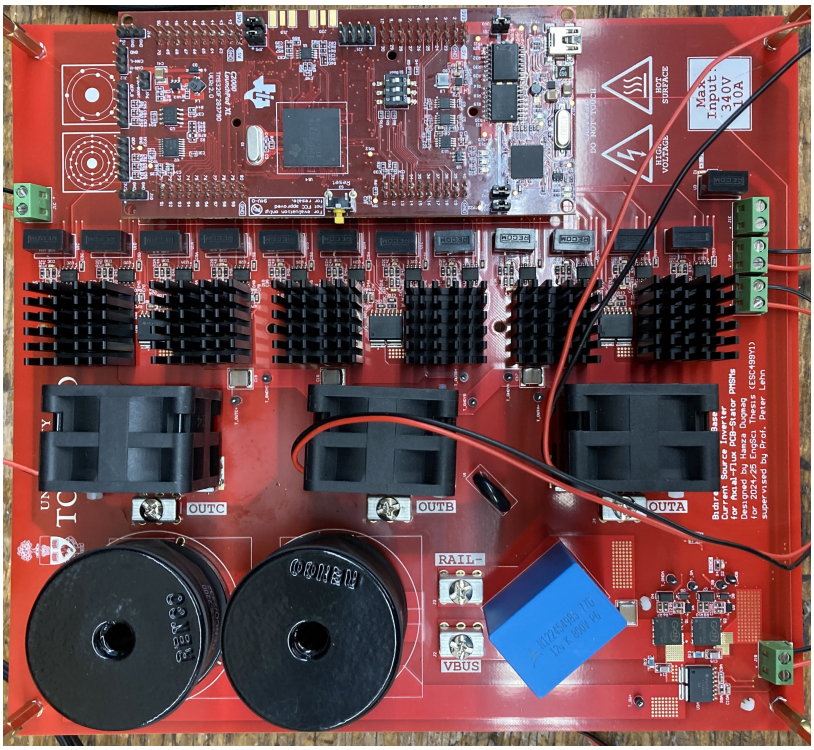

Figure 3.16: Top-layer of the fully assembled PCB.

three top gating signals as well as the three bottom gating signals. A path for the DC link current always needs to be present, so at any moment, at least one top and one bottom switch in the CSI leg need to be conducting (while avoiding interphase short-circuit) [42]. To reduce filter capacitor voltage ripple, a symmetrical modulation method from [40, 41] is used to arrange the sequence of switching states in a switching period. Note that D_d is the same as m_a here.

As mentioned, there are three approaches to implement reverse-blocking capability from the BD switches. Since the IGLT65R055B2 is equivalent to two source-connected sub-switches, the equivalent body diode of the top sub-switch is leveraged to reverse block. Therefore, the first approach is to add a 0 Ω resistor shorting G2 to KS2. This reduces cost (half as many gate drivers needed) as well as reverse conduction loss since $V_{gs,2} = 0$ V, however it increases the risk of mis-triggering since this voltage is close to the threshold voltage (less stable turn-off). The second approach is the four-step modulation scheme. Although this theoretically reduces conduction loss more than it increases switching loss (to be validated), the complex gating scheme risks interphase shorts. Also, it is not compatible with the *PLECS* file (custom firmware needs to be programmed, which will take time).

Therefore, for the purpose of this first prototype, we de-risk our experiments by holding $V_{gs,2} = -3$ V via a dedicated gate driver. This does deteriorate efficiency by increasing reverse conduction loss (the voltage drop across the equivalent diode is ≈ 3 V), but the purpose of our initial tests is to verify the CSI operation, so this trade-off is acceptable. Therefore, in *PLECS*, our PWM blocks are configured to single-output mode (PWM channel A only), implying that the bottom sub-switches are gated with SVPWM while the gating signals for the top sub-switches are held low (PWM channel B). Referring to Figure 3.2, all the bottom sub-switches are driven by channel A of the DSP's PWM modules except for switches C+ and A- (they are driven by channel B instead to reduce layout inductance). Therefore, in *PLECS*, the corresponding PWM blocks should be configured to dual-output mode (PWM channel A and B driven independently), where channel A is held low and channel B is gated. Unfortunately, after assembling the board, we discovered that a bug in *PLECS* prevents driving channel B independently. To avoid wasting time trying to program the firmware manually, a workaround is implemented as follows:

1. Referring to Figure 3.2, cut the male headers on the PCB that connect to the DSP's PWM1A (connects to PWMA2- on the PCB) and PWM6A (connects to PWMC2+ on the PCB) pins.

2. On the bottom layer of the PCB, short PWMA2- and PWMC2+ to ground by soldering a wire (keeps the top sub-switches off).

3. Short PWM1A to PWM1B and PWM6A to PWM6B using two-pin jumpers on the DSP's male headers.

4. Issue the SVPWM signals to PWM1A and PWM6A instead, hence driving PWMA1- and PWMC1+ (now we can use single-output mode in *PLECS*, which is functional).

The downside with this approach is that since the PWMA2- and PWMC2+ are physically tied to ground, four-step commutation cannot be implemented. One would need to de-solder the ground connections, replace the cut headers, and manually program the dual-output mode configuration for the PWM blocks.

If the switches were actually equivalently drain-connected (bottom sub-switch should be off), then there will not be any output current because the effective body diodes would always be reverse biased (I_{dc} cannot be < 0 A because we're using a buck front-end). There is no risk of damaging the switches if we're accidentally

driving the wrong sub-switch. However, resolving this issue will entail having to do the same as what was done with switches C+ and A- for all the other switches (this time, C+ and A- will be driven in single-output mode).

In terms of DC current regulation with the buck converter, for some reason, the peak current control block only supports single-output mode operation, not complementary output (although the option for complementary output is available). Using single-output mode in a synchronous buck converter should regulate the current just fine since it would leverage the lower body diode, but at reduced efficiency and with a risk of burning out the bottom switch. Therefore, due to limited time available to implement my own peak current or PI controller, a rudimentary hysteretic current control is used to verify operation. To avoid risking burning out the switches, the on and off duty cycles are 95% and 5% respectively (instead of 100% and 0%). The ADC channel reading the output of the I_{dc} Hall sensor is calibrated at zero current after averaging the measurement arbitrarily for five seconds. Assuming the sensitivity is as mentioned in the datasheet (100 mV/A), only the offset is adjusted. For this sensor, it was changed from -16.5 to -16.76.

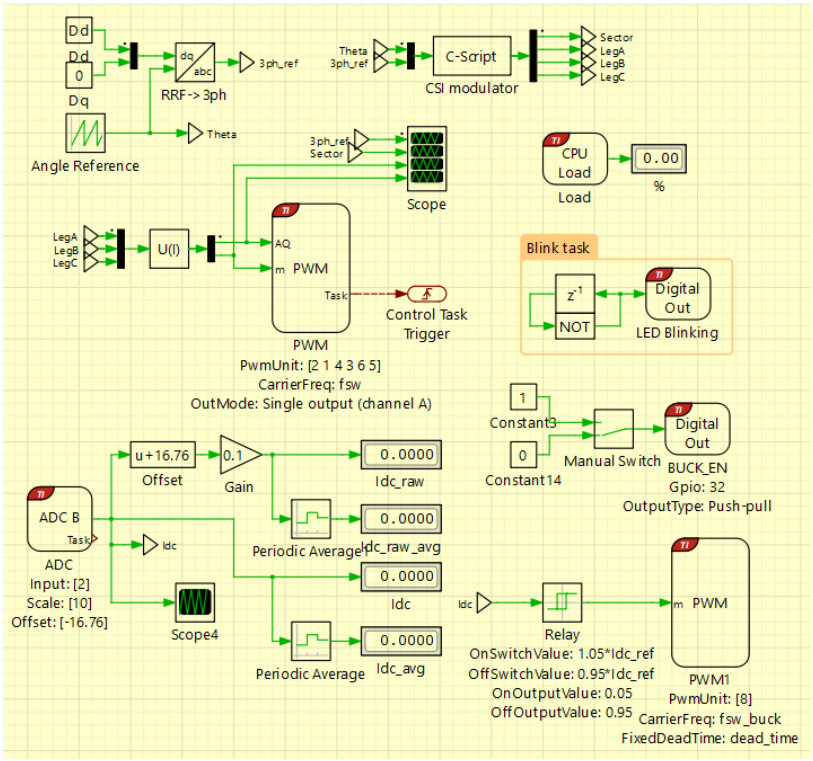

Figure 3.17: *PLECS* firmware for the C2000 DSP for CSI and buck control.

Chapter 4

Results and Discussion

4.1 Experimental Setup

For this thesis, there are two experiments to validate the operation of both the CSI and buck converter. First, in Section 4.3, the buck converter will be bypassed by connecting the power supply (set to constant current mode) to the switch node (a wire is soldered to the copper pad next to Q1 in Figure 3.13). This will allow us to confirm the SVPWM signals are issued correctly and that the CSI is inverting the DC current correctly. After ensuring the CSI works, we can introduce I_{dc} regulation by enabling the buck converter and connecting the power supply (as a DC voltage source) to the input terminals, as in Section 4.4.

To prevent the risk of damaging the switches (overcurrent, overvoltage, overheating), the tests will be conducted at low power ($\leq$ 30 V and 1 A input). Although the typical load in a real application would be inductive (e.g., PCB-stator AFPMSM), we avoid potential resonance and overvoltage failures with the filter capacitors by driving a three-phase Wye-connected resistor instead. Since the filter capacitor voltage is proportional to the output phase current and load resistance, using a small phase resistance will allow us to satisfy the input voltage requirement. Otherwise, a larger load will require a larger input voltage to drive the same output phase currents. Here, we measure 12.2 Ω between lines, so the phase resistance is 6.1 Ω. At the worst case switching frequency (50 kHz), the CSI example design in *PLECS* is simulated (no buck converter) to confirm that the output current and voltage ripples would be low enough at $I_{dc} \leq 1$ A to verify inversion experimentally by inspection. A modulation ratio less than 1 is temporarily used to avoid any potential comparator errors.

Table 4.1: *PLECS* simulation parameters to confirm experimental circuit parameters.

Parameter	Value
f_s	50 kHz
f_e	50 Hz
V_{in}	5 V
m_a	0.8
L_{dc}	1.1 mH
C_f	2.2 μF
R_{load}	6.1 Ω

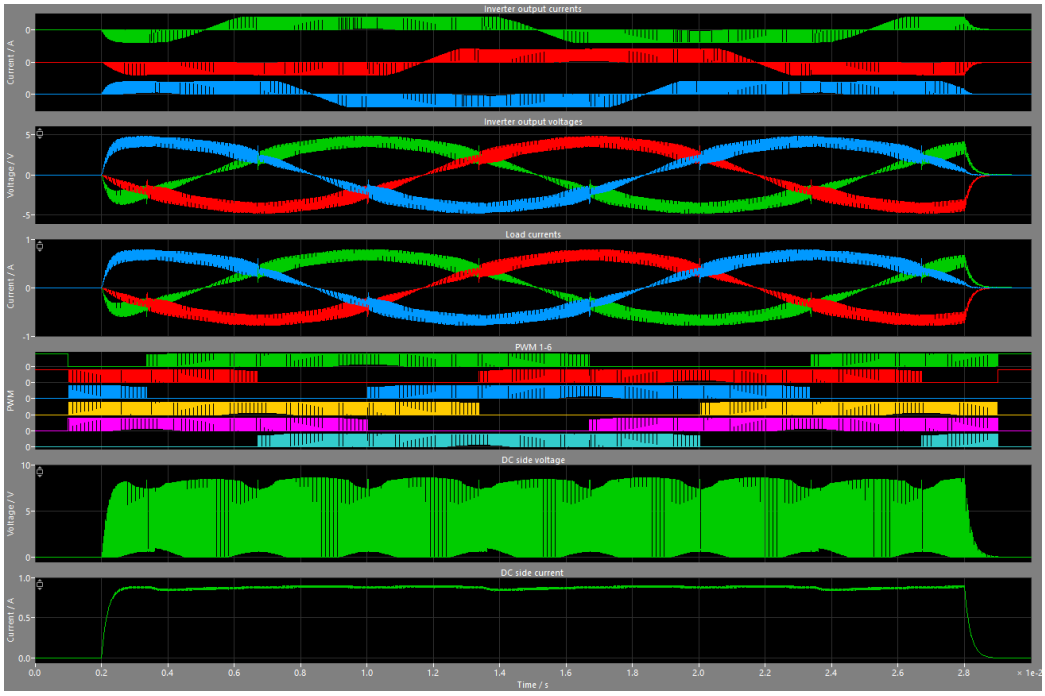

Figure 4.1: *PLECS* simulation waveforms.

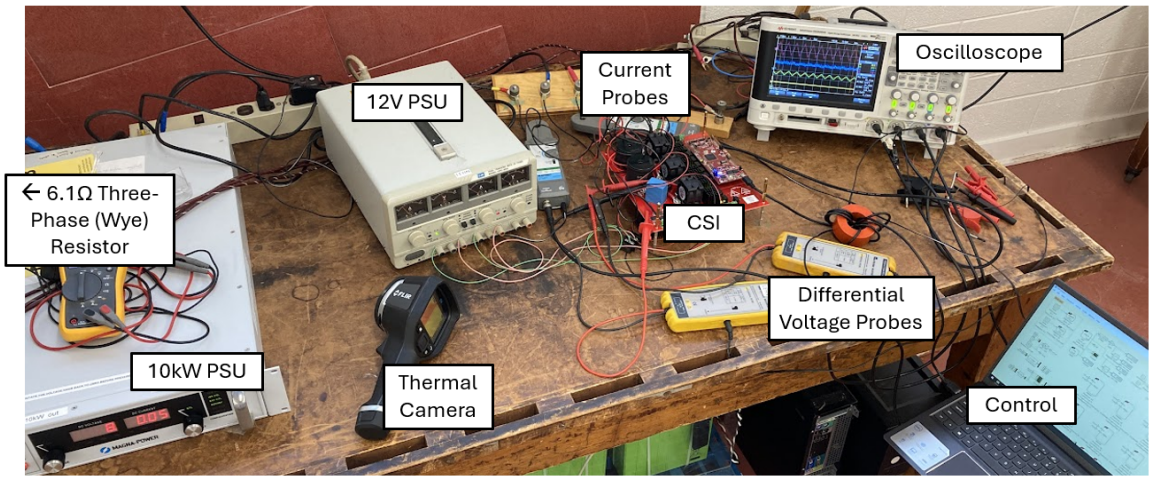

Figure 4.2: Experimental setup for driving a three-phase resistive load.

Differential voltage probes are used to avoid shorting nodes together when probing multiple signals. The current probes are calibrated at zero current before turning the power supply on. The DC link inductor voltage is monitored to ensure there are no voltage spikes that would otherwise indicate incorrect SVPWM signals. The DC link inductor current is also probed to observe how the DC link current is regulated, either by the power supply in constant current mode or by the buck converter. CSI operation is validated by probing the output phase currents and filter capacitor voltages (line to neutral). The USB cable connecting the laptop to the DSP is wound around an iron core to mitigate EMI, especially when using external mode to read the DC link inductor directly in *PLECS*.

4.2 Gate Driving

The 12 V auxiliary supply is powers the gate drivers and Hall sensors through the isolated DC-DC converters. Dead time for the buck converter is verified by probing the two gating signals with the oscilloscope. On the other hand, live time for the CSI is verified by probing the three top gating signals, and the three bottom gating signals, skimming through the six sectors to ensure at least one switch is always on. We start testing at very low DC link current (50 mA limit on the power supply) just in case the live time requirement is violated in any of the thousands of switching periods in a full cycle. This ensures any voltage spiking across L_{dc} is well below the rated voltage of the switches (650 V) and the varistor is not stressed.

Table 4.2: Auxiliary power verification measurements.

Parameter	**Measurement**	**Comments**
Supply Voltage	12 V	
Supply Current	0.6 A	$P_{\text{aux}} = 7.2$ W
12V/3V3 Converter Output	3.466 V	
12V/12V Converter Output	12.33 V	
BD-GaN Turn-Off Voltage (V_{EE})	-2.941 V	Designed for -3 V
BD-GaN Turn-On Voltage (V_{DD})	9.36 V	Designed for +9 V

4.3 Constant Current Supply

With no input power supplied, the voltage across the input terminals was measured to be around 8 V. This is attributed to the reverse conduction voltage drops when driving the top sub-switches at a negative turn-off voltage. After confirming no L_{dc}

voltage spikes at I_{dc} = 50 mA, the current limit was swept up to 1 A. To avoid sudden I_{dc} interruption during shutdown or changing the firmware, the input power supply voltage is dialed down all the way to the left until I_{dc} naturally falls to 0 A as the output capacitor voltage discharges L_{dc}.

Table 4.3: Experimental parameters under a constant current power supply.

Parameter	**Value**
f_e	50 Hz
f_s	40 kHz
m_a	0.8
D_{live}	4%

Table 4.4: Input current and corresponding terminal voltage under a constant current power supply.

Current Limit (I_{dc}) [mA]	**Input Terminal Voltage (V_{in}) [V]**
0	7.72
50	8.51
100	8.85
200	9.39
300	9.98
400	10.60
500	11.24
600	11.82
700	12.46
800	13.07
900	13.69
1000	14.31

Table 4.5: Fourier analysis under constant current supply of Figure 4.4. Total harmonic distortion is calculated on 3000 harmonics of 50 Hz.

Signal	**Total Harmonic Distortion**	**DC Component**
$I_{out,a}$	23.27%	0.0357 A
$V_{Cf,a}$	24.12%	6.996 V

This experiment successfully outputs a three-phase balanced sinusoidal current at the expected magnitude according to Figure 4.3: $\frac{565.1 \text{ mArms} \cdot \sqrt{2}}{0.8}$ = 998.97 mA. Additionally, the output filter capacitor produces a sinusoidal output voltage with the expected amplitude ($\frac{3.417 \text{ Vrms}}{0.5651 \text{ Arms}} = 6.05\ \Omega$), proving the benefits in terms of harmonic spectrum of the CSI over the VSI. The DC offset is attributed to the effective body diode voltage drops when driving at negative turn-off gate voltage. The fairly

high total harmonic distortions (THD) is because f_s is below specification and that the load is purely resistive. Driving an inductive load like a PCB-stator AFPMSM should decrease the output phase current ripple as the stator inductance filters out the current.

From Figure 4.4, the DC link inductor is constant, with a peak-to-peak ripple of 600 mA. There are no voltage spikes across the inductor, proving that live time is implemented correctly within the SVPWM scheme. The hottest components during operation were the CSI gate drivers. At $f_s = 40$ kHz, the temperature peaked at 73.5 °C, which is fairly high. If we ever want to increase the switching frequency, then care needs to be taken since power dissipation is dependent to f_s [124]. At $I_{out,a} = 0.8$ A, the heatsink temperatures were around 44.5 °C, which is reasonable considering the fans were not turned on.

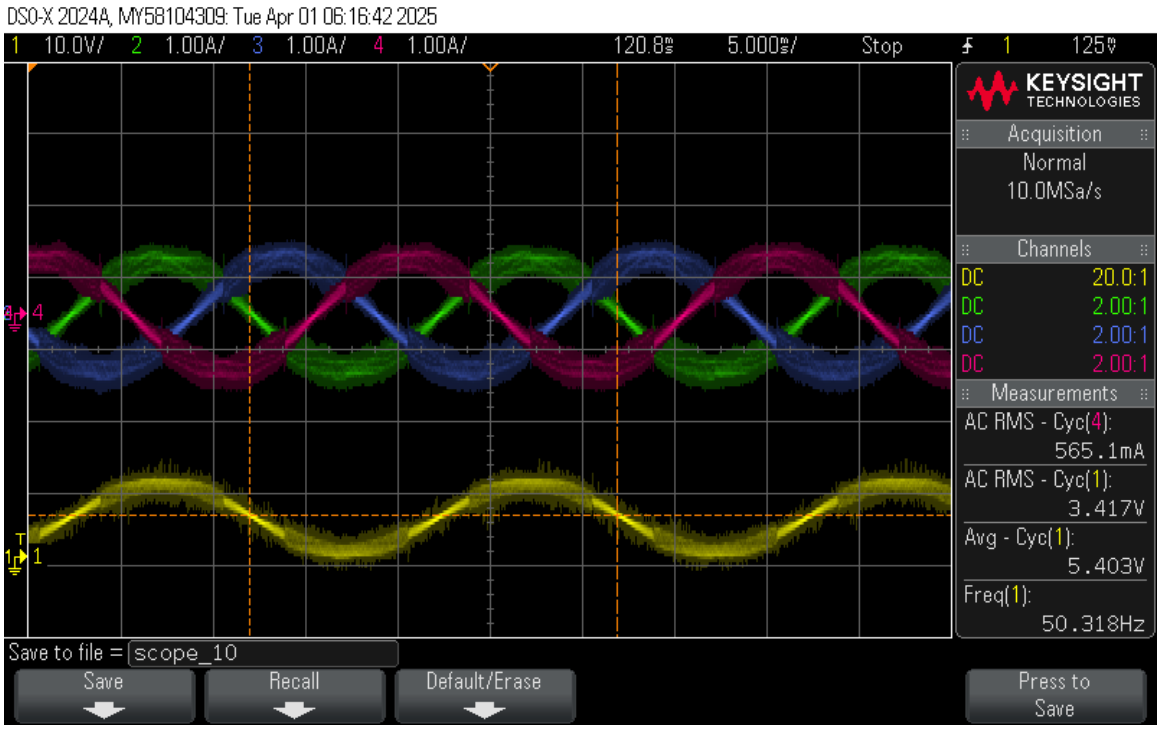

Figure 4.3: Three-phase output of the prototype board under constant current supply at $I_{dc} = 1$ A (yellow: $V_{Cf,a}$, green: $I_{out,a}$, blue: $I_{out,b}$, pink: $I_{out,c}$).

4.4 Buck Converter

Although using the buck converter does regulate the DC link current and outputs sinusoidal currents and voltages, the DC link current ripple is large, hence distorting

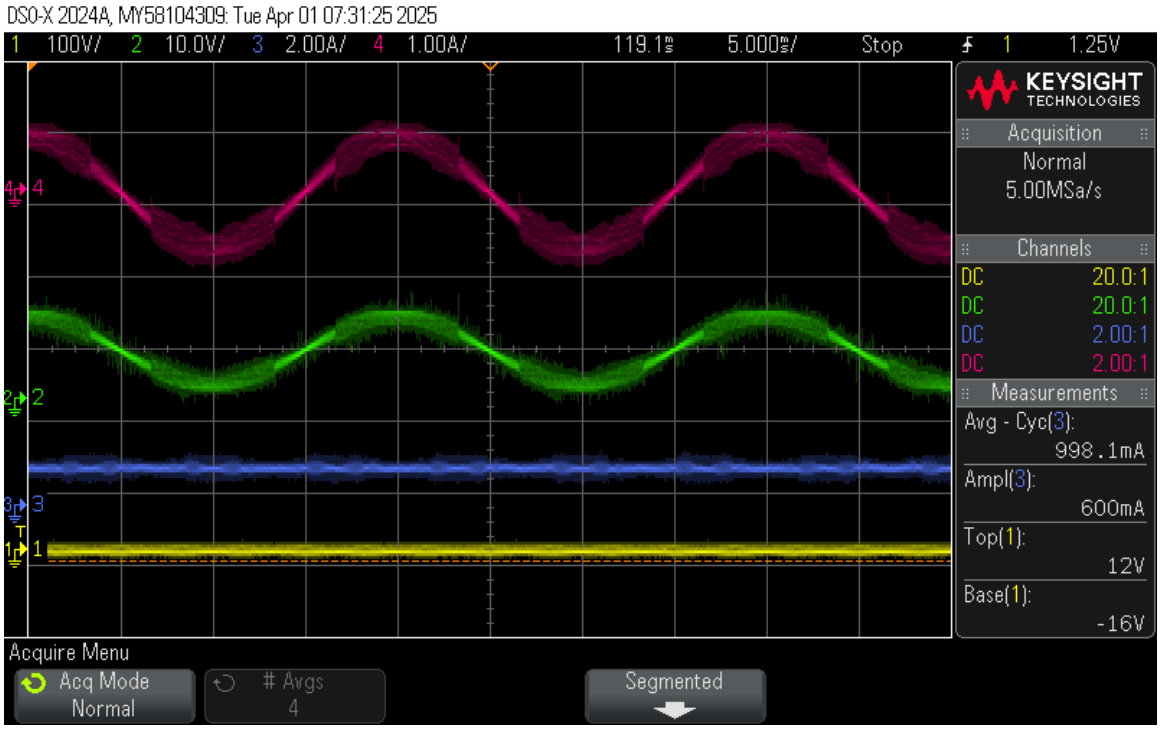

Figure 4.4: Phase A and input voltages and currents under constant current supply at $I_{dc} = 1$ A (yellow: V_{Ldc}, green: $V_{Cf,a}$, blue: I_{dc}, pink: $I_{out,a}$).

Figure 4.5: Thermal measurement of the CSI gate drivers and heatsinks at $I_{dc} = 1$ A and $f_s = 40$ kHz under constant current supply.

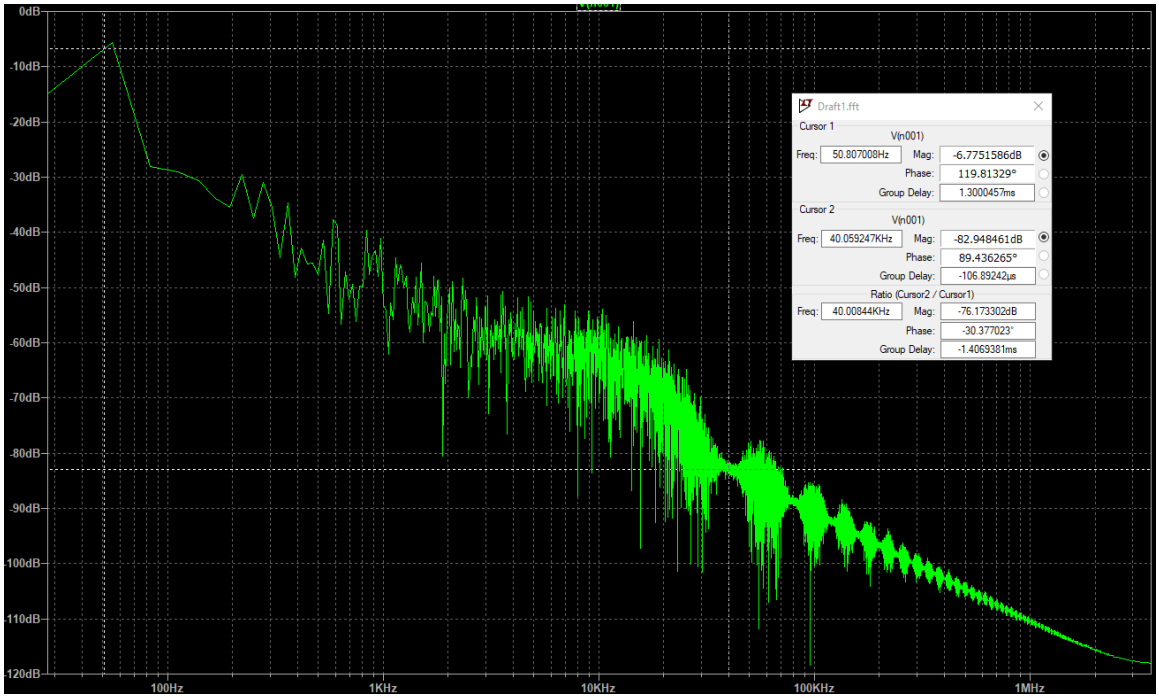

Figure 4.6: Fourier transform of $I_{out,a}$ under constant current supply from Figure 4.4.

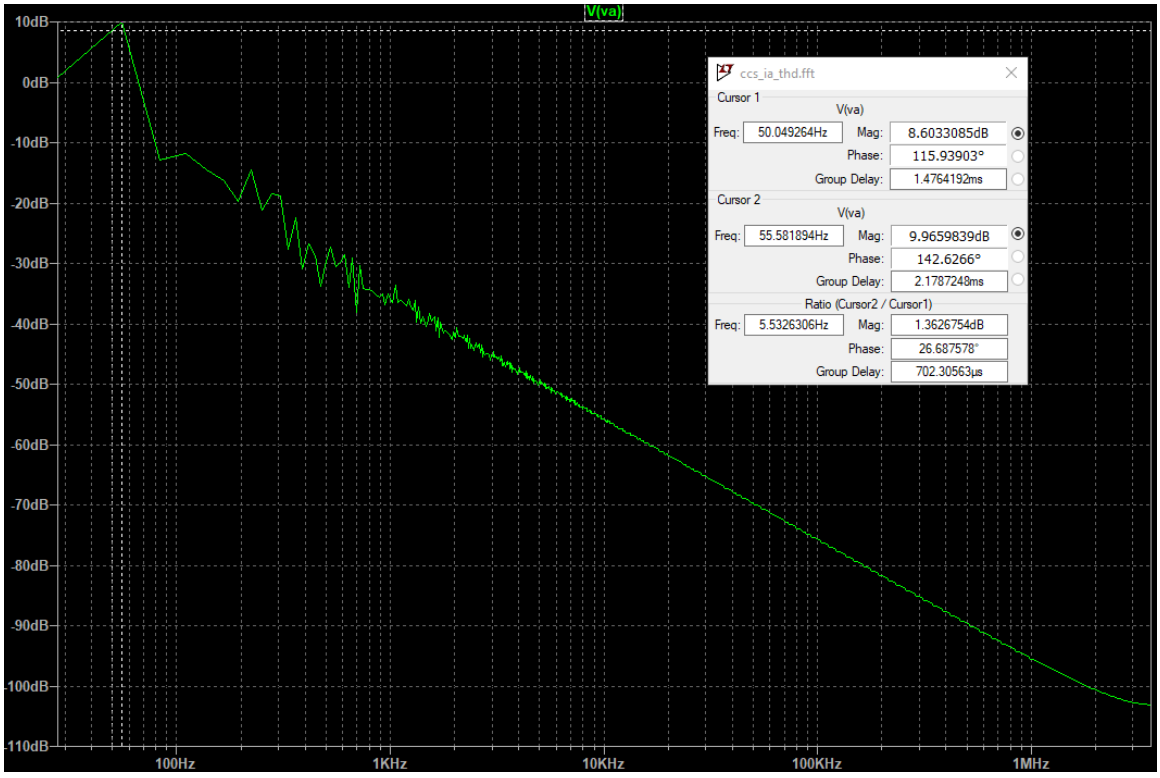

Figure 4.7: Fourier transform of $V_{Cf,a}$ under constant current supply from Figure 4.4.

Table 4.6: Experimental parameters when operating with the buck converter enabled.

Parameter	**Value**
f_e	50 Hz
f_s	40 kHz
f_{buck}	100 kHz
I_{ref}	700 mA
m_a	0.8
D_{live}	4%

Table 4.7: Fourier analysis under buck converter operation of Figure 4.10. Total harmonic distortion is calculated on 3000 harmonics of 50 Hz.

Signal	**Total Harmonic Distortion**	**DC Component**
$I_{out,a}$	24.94%	−0.0347 A
$V_{Cf,a}$	25.92%	5.632 V

the output waveforms as well (worse THD than under constant current supply). The ripple is roughly equal to the reference current. This is attributed to the fact that the hysteretic current controller is too slow. The RC filter at the Hall sensor has a bandwidth of 1.59 kHz, which is over two orders of magnitude smaller than the buck's switching frequency. Also, using hysteretic current control with an off-duty of 5% causes I_{dc} to drop much faster than the controller can respond. According to Figure 4.9, this causes the circuit to enter discontinuous conduction mode as I_{dc} drops to 0 A periodically.

Nevertheless, for the same $I_{ref} = 700$ mA, the buck converter is able to limit the current across a wide range of V_{in} (tested from 13 V to 30 V). However, due to the slow controller, the distortion increases as V_{in} does (as evident by comparing the waveforms in Figures 4.8 and 4.10). The hottest components were still the CSI gate drivers, with the buck converter switches still at room temperature.

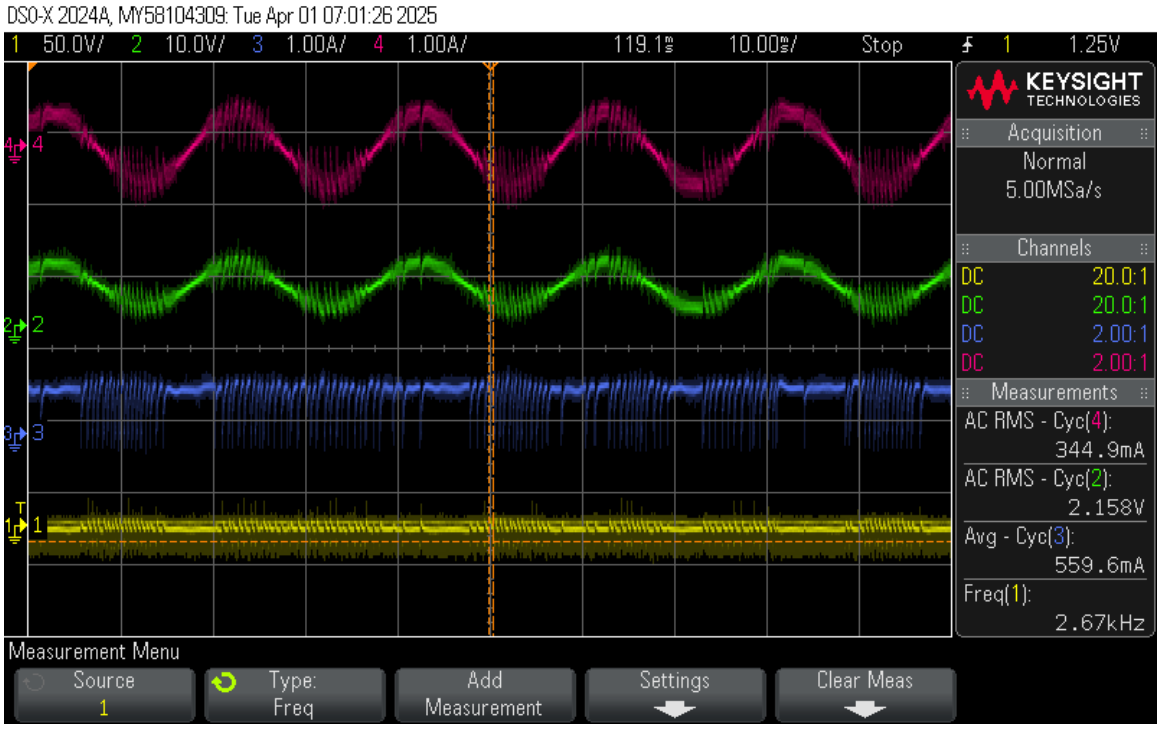

Figure 4.8: Phase A and input voltages and currents under buck converter operation with $V_{in} = 13$ V (yellow: V_{Ldc}, green: $V_{Cf,a}$, blue: I_{dc}, pink: $I_{out,a}$).

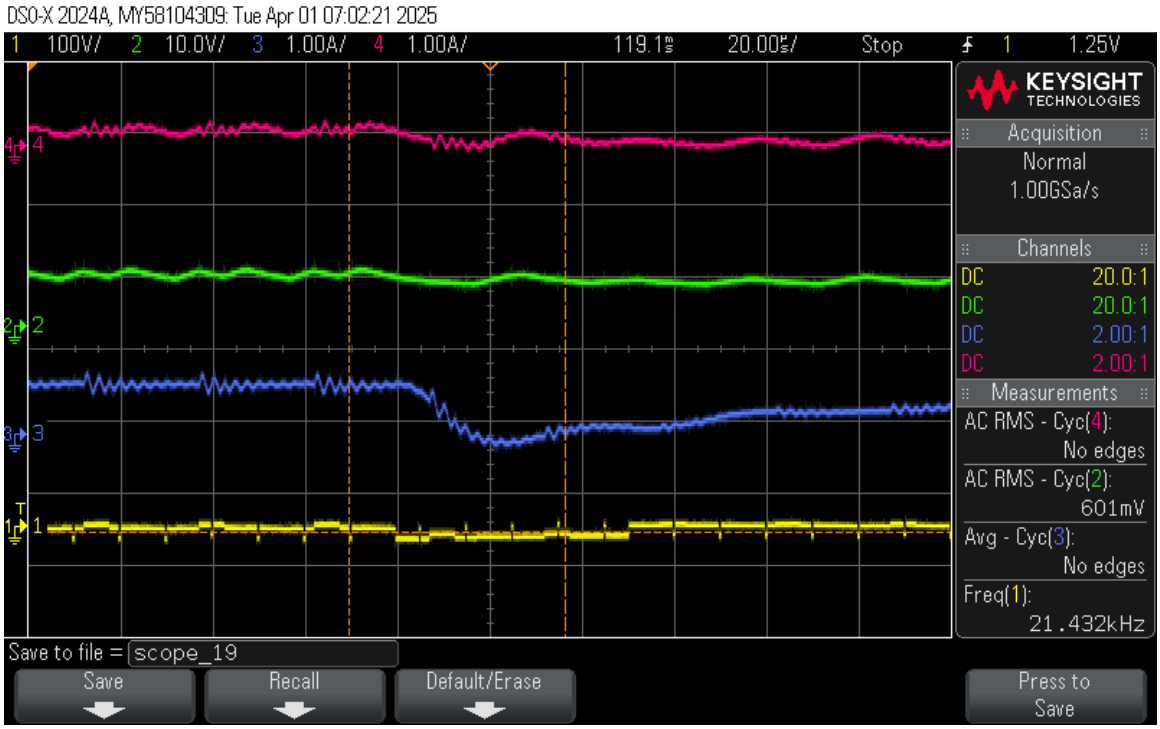

Figure 4.9: Zoom into Figure 4.8 to observe buck response to I_{dc}.

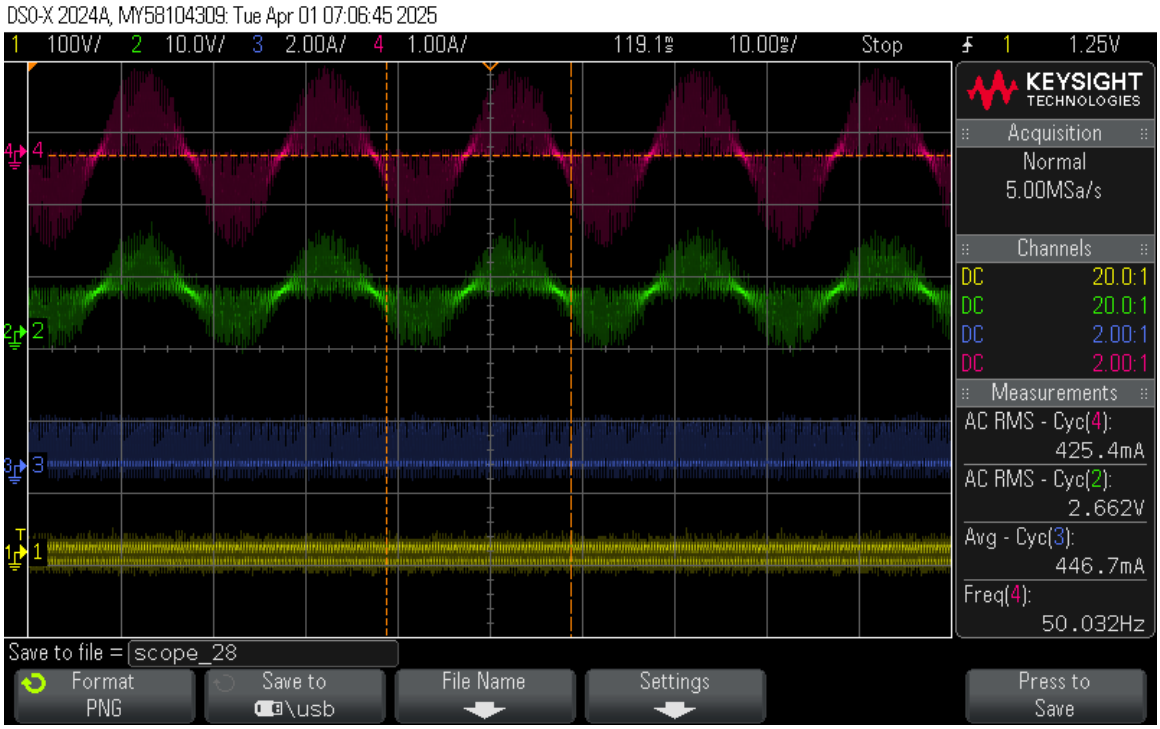

Figure 4.10: Phase A and input voltages and currents under buck converter operation with $V_{in} = 20$ V (yellow: V_{Ldc}, green: $V_{Cf,a}$, blue: I_{dc}, pink: $I_{out,a}$).

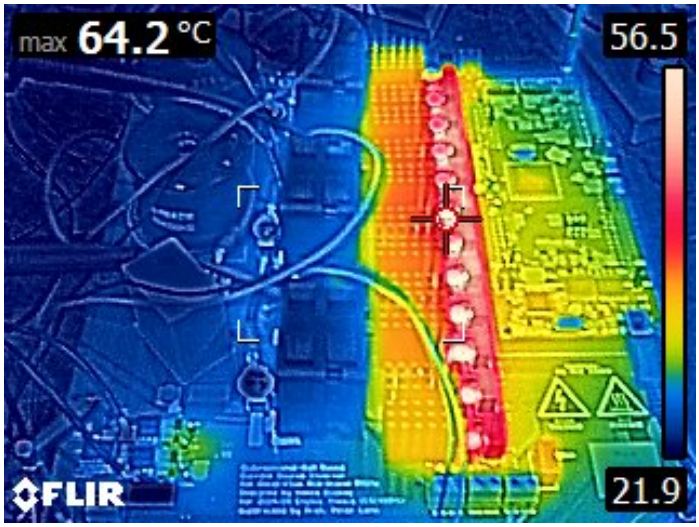

Figure 4.11: Thermal measurement of the prototype board at $I_{ref} = 700$ mA and $f_s = 40$ kHz under buck converter operation.

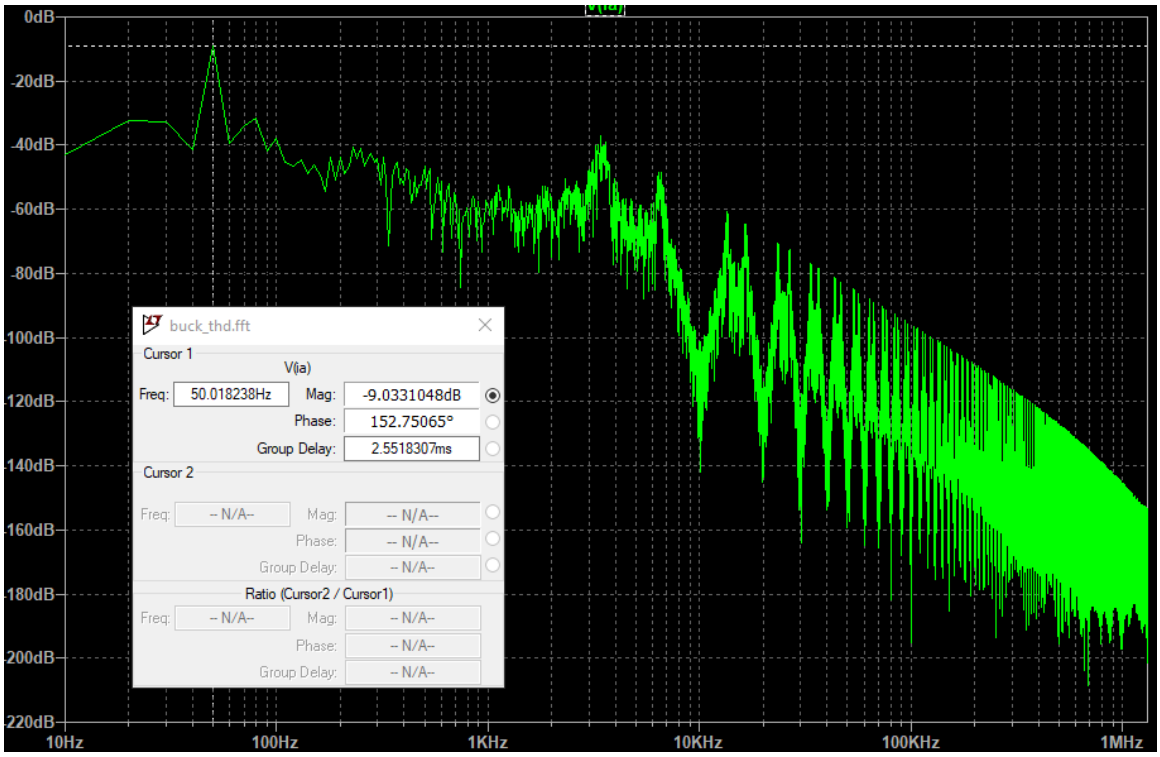

Figure 4.12: Fourier transform of $I_{out,a}$ under buck converter operation from Figure 4.10.

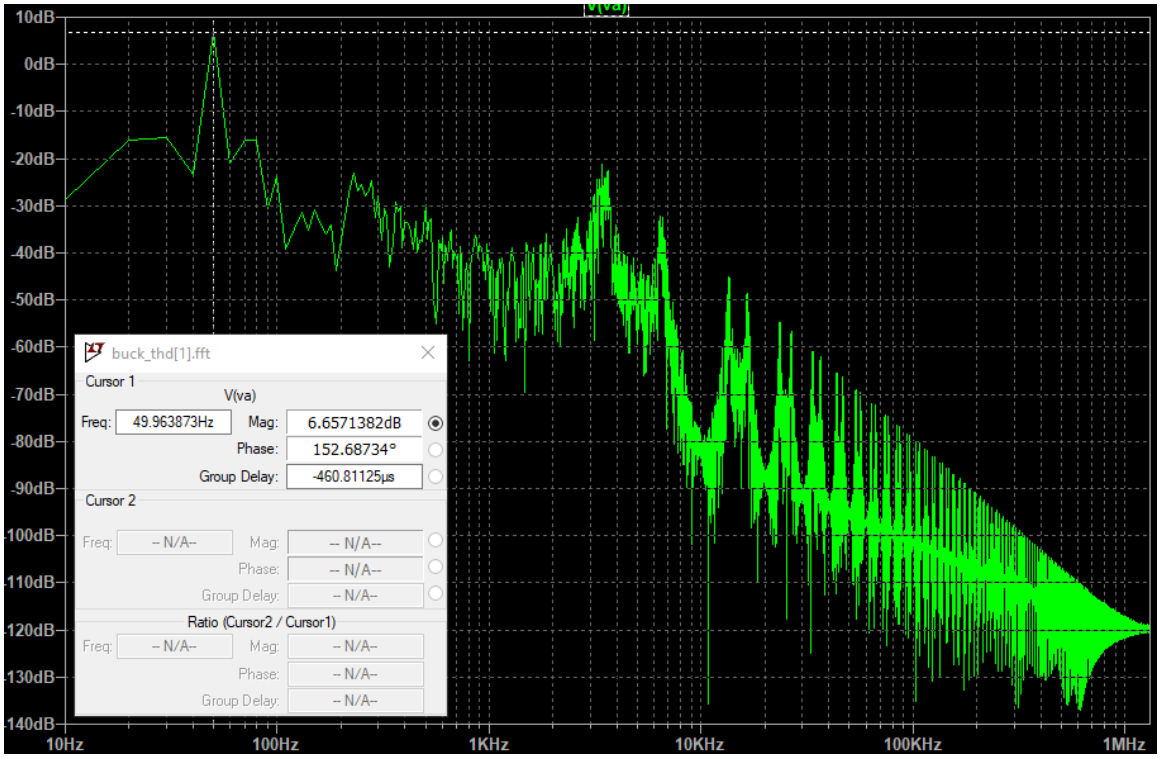

Figure 4.13: Fourier transform of $V_{Cf,a}$ under buck converter operation from Figure 4.10.

Chapter 5

Conclusion and Future Work

5.1 Significance

Overall, this thesis project successfully demonstrates the deployment of the IGLT65R055B2 monolithic bidirectional GaN switch in CSIs. This project highlights key design practices with regards to the circuit parameters, schematic, and layout, all justified by successful validation of the prototype board driving a three-phase resistive load. This project paves the way for future investigations towards making the case for adopting CSIs in motor drive applications, especially with the advent of these new bidirectional devices and low-inductance electric machines.

5.2 Design Improvements

This thesis serves as a first iteration of investigating the application and design of bidirectional GaN in CSIs. As such, several improvements have been identified for future improvement of the inverter's performance, reliability, and capability:

- There is an opportunity to increase the output filter capacitance by using stacked ceramic capacitors with mounting brackets [116]. Not only would this reduce output voltage ripple and parasitic inductance for a very low cost, but the footprint can be made smaller. This improves structural reliability, especially in motor applications where vibrations can cause cracking in large capacitors and soldered connections.
- To investigate four-step commutation, the physical PCB changes done in Section 3.5 need to be reversed, as outlined in that section.

- To better regulate I_{dc}, increase the RC filter bandwidth at the I_{dc} Hall sensor output and implement peak current or PI control (better performance than hysteretic control).
- To enable position-sensorless control of PMSMs using this CSI, output voltage sensors must be added.
- Test points to probe the gate voltages of the BD-GaN devices should be added. Care should be taken to avoid increasing parasitic layout inductance, as highlighted in [125]. Consider having them pointing through the bottom layer of the PCB since there might not be enough room on the top layer.
- The thermal and mechanical assembly was tedious. Increasing the heatsink mounting hole size, separation, and count allows for a safer (insulated) and more robust heatsinking solution for the BD-GaN devices. Also, considering how the fans will be mounted and adding enough clearance to attach screws and nuts will improve structural reliability and facilitate the assembly process.
- A toggle switch should be added for the fans.

5.3 Motor Drive

After validating the CSI operation under a fixed RL load, the next step would be to enable the prototype as a PCB-stator AFPMSM motor drive. The first experiment is the blocked-rotor test, with the objective of characterizing *Celestica*'s motor losses when driven by a VSI and CSI at the same switching frequency and fundamental ($f_e = 60$ Hz) phase current magnitude at $m_a = 1$. Per the PCB design requirements, the DC link current will go up to 10 A while the switching frequency ranges from 50 kHz to 200 kHz. When the rotor is blocked (zero speed), the useful mechanical power and mechanical losses (bearing friction) are zero. Therefore, any power fed to the motor from the inverter goes towards Joule, eddy, and hysteresis losses inside the motor. Thus the test setup consists of the inverter (VSI or CSI) connected to the motor with its rotor locked securely. The DC bus voltage and 12 V auxiliary power will be supplied externally. Since no speed voltage is induced and the phase currents are responsible for the loss mechanism, the DC bus voltage may be lowered below 340 V. A *Hioki* PW6001A961-09 power analyzer will be connected to the output terminals of the inverter, phase locked at the switching and fundamental frequencies.

When the motor spins during nominal operation, the losses in the rotor magnets (hysteresis and eddy) at f_e are eliminated as they experience no changing reluctance or magnetic field. Therefore, the blocked-rotor test is expected to overestimate the losses at f_e, especially since the magnets are unlaminated [3, 59]. Since the coreless design of the PCB-stator AFPMSM already eliminates most losses, it is hypothesized that only marginal motor efficiency improvements may be obtained by using a CSI over a VSI. Losses would increase at lower switching frequencies (more unattenuated harmonics) and higher currents, so the greatest difference between driving the motor with a VSI and CSI would be observed at these operating conditions.

The second experiment would be to characterize the CSI performance by measuring its efficiency at different f_s, f_{buck}, m_a, and I_{dc} while the motor is spinning at nominal speed. The efficiency is hypothesized to peak at some power level, trailing off in both directions. At low input power, most of it will be used to supply the gate drivers and Hall sensors, which is roughly constant. As the DC bus input power increases and the auxiliary power stays the same, a larger portion of the total input power is transferred to the output, with low switching and conduction losses because the current is relatively small. As I_{dc}, and hence input power at constant DC input voltage, increases, switching and conduction losses will increase, lowering the efficiency [126]. Characterizing and comparing the losses between four-step commutation and permanently keeping the top sub-switch in diode mode at $V_{gs} = 0$ V may also be investigated.

To measure the efficiency here, the power analyzer will be connected to the input and output terminals of the CSI. The DC power of the auxiliary 12 V supply can be measured from the voltage and current readings on its power supply. The drive can operate in open-loop (except for I_{dc} regulation) or in closed-loop if output voltage sensors are added. In the former, the fundamental frequency of the phase currents will be programmed to slowly increase up to 60 Hz as the rotor safely accelerates and locks on [127]. The motor's efficiency (hence the total machine loss) may be extracted by connecting it to a dynamometer [128]. The efficiency of an inverter depends on various factors (modulation scheme, switch specifications, etc.), so it is not fruitful to compare our CSI efficiency to that of *Celestica*'s VSI.

Bibliography

[1] International Energy Agency, "World Energy Outlook 2016," November 2023. [Online]. Available: https://iea.blob.core.windows.net/assets/680c05c8-1d6e-42ae-b953-68e0420d46d5/WEO2016.pdf

[2] S. D. Umans, *Electric Machinery*, 7th ed. New York: McGraw-Hill, 2014.

[3] P. Guedes-Pinto, "An Axial-Flux Motor for an Electrified World: It Combines the Best of Two Motor Designs to Save Weight and Energy," *IEEE Spectrum*, vol. 59, no. 4, pp. 38–43, 2022.

[4] H. Dai and T. M. Jahns, "Comparative investigation of PWM current-source inverters for future machine drives using high-frequency wide-bandgap power switches," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2601–2608.

[5] M. Buffolo, D. Favero, A. Marcuzzi, C. De Santi, G. Meneghesso, E. Zanoni, and M. Meneghini, "Review and Outlook on GaN and SiC Power Devices: Industrial State-of-the-Art, Applications, and Perspectives," *IEEE Transactions on Electron Devices*, vol. 71, no. 3, pp. 1344–1355, 2024.

[6] Infineon Technologies, "Infineon announces CoolGaN™ bidirectional switch and CoolGaN Smart Sense for higher performance and more cost-effective power systems," Jun 2024. [Online]. Available: https://www.infineon.com/cms/en/about-infineon/press/market-news/2024/INFPSS202406-111.html

[7] M. Guacci, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, "Novel Three-Phase Two-Third-Modulated Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs," in *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2019, pp. 674–683.

[8] United Nations, "Paris Agreement," 2015. [Online]. Available: https://unfccc.int/sites/default/files/english_paris_agreement.pdf

[9] International Energy Agency, "World Energy Outlook 2023," October 2023. [Online]. Available: https://iea.blob.core.windows.net/assets/86ede39e-4436-42d7-ba2a-edf61467e070/WorldEnergyOutlook2023.pdf

[10] ——, "World Energy Outlook 2024," October 2024. [Online]. Available: https://iea.blob.core.windows.net/assets/60db7f34-da7f-41d7-8232-c0b718463fd0/WorldEnergyOutlook2024.pdf

[11] Lopez, Nuria, "Copernicus: 2024 is the first year to exceed 1.5°C above pre-industrial level," January 2025. [Online]. Available: https://climate.copernicus.eu/copernicus-2024-first-year-exceed-15degc-above-pre-industrial-level

[12] International Energy Agency, "World Energy Outlook 2022," October 2022. [Online]. Available: https://iea.blob.core.windows.net/assets/830fe099-5530-48f2-a7c1-11f35d510983/WorldEnergyOutlook2022.pdf

[13] A. De Almeida, J. Fong, C. Brunner, R. Werle, and M. Van Werkhoven, "New technology trends and policy needs in energy efficient motor systems - A major opportunity for energy and carbon savings," *Renewable and Sustainable Energy Reviews*, vol. 115, p. 109384, 2019. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1364032119305921

[14] N. S., S. P. Nikam, S. Pal, A. K. Wankhede, and B. G. Fernandes, "Performance Comparison Between PCB-Stator and Laminated-Core-Stator-Based Designs of Axial Flux Permanent Magnet Motors for High-Speed Low-Power Applications," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 7, pp. 5269–5277, 2020.

[15] Y. Chulaee, G. Heins, B. Robinson, A. Mohammadi, M. Thiele, D. Patterson, and D. M. Ionel, "Design and Optimization of High-Efficiency Coreless PCB Stator Axial Flux PM Machines with Minimal Eddy and Circulating Current Losses," *IEEE Transactions on Industry Applications*, pp. 1–13, 2024.

[16] Y. Li, D. Han, N. Altintas, and B. Sarlioglu, "Design of high-speed toroidal winding surface PM machine with SiC-based inverters," in *2016 XXII International Conference on Electrical Machines (ICEM)*, 2016, pp. 1559–1565.

[17] A. K. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy, and H. A. Toliyat, "Wide Bandgap Devices in AC Electric Drives: Opportunities and Challenges," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 1, pp. 3–20, 2019.

[18] K. Vogel and A. J. Rossa, "Improving Efficiency in AC drives: Comparison of Topologies and Device Technologies," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2014, pp. 1–8.

[19] A. Morya, M. Moosavi, M. C. Gardner, and H. A. Toliyat, "Applications of Wide Bandgap (WBG) devices in AC electric drives: A technology status review," in *2017 IEEE International Electric Machines and Drives Conference (IEMDC)*, 2017, pp. 1–8.

[20] J. Wang, V. Veliadis, J. Zhang, Y. Alsmadi, P. R. Wilson, and M. J. Scott, "IEEE ITRW Working Group Position Paper-System Integration and Application: Silicon Carbide: A Roadmap for Silicon Carbide Adoption in Power Conversion Applications," *IEEE Power Electronics Magazine*, vol. 5, no. 2, pp. 40–44, 2018.

[21] D. Han, S. Li, W. Lee, and B. Sarlioglu, "Adoption of wide bandgap technology in hybrid/electric vehicles-opportunities and challenges," in *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2017, pp. 561–566.

[22] A. I. Emon, M. ul Hassan, A. B. Mirza, J. Kaplun, S. S. Vala, and F. Luo, "A Review of High-Speed GaN Power Modules: State of the Art, Challenges, and Solutions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 2707–2729, 2023.

[23] W. Lee, D. Han, and B. Sarlioglu, "GaN-based single phase brushless DC motor drive for high-speed applications," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, 2014, pp. 1499–1505.

[24] O. Gulsuna, F. Tokgoz, F. Karakaya, and O. Keysan, "Design and Analysis of a GaN-Based Megahertz Integrated Motor Drive for a PCB Motor," *IEEE Transactions on Industrial Electronics*, pp. 1–10, 2024.

[25] C.-M. Liang, Y.-J. Lin, J.-Y. Chen, G.-R. Chen, and S.-C. Yang, "Sensorless LC Filter Implementation for Permanent Magnet Machine Drive Using

Observer-Based Voltage and Current Estimation," *Sensors*, vol. 21, no. 11, 2021. [Online]. Available: https://www.mdpi.com/1424-8220/21/11/3596

[26] E. P. Wiechmann, P. Aqueveque, R. Burgos, and J. Rodriguez, "On the Efficiency of Voltage Source and Current Source Inverters for High-Power Drives," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 4, pp. 1771–1782, 2008.

[27] G. L. Fidone, G. Migliazza, E. Carfagna, D. Benatti, F. Immovilli, G. Buticchi, and E. Lorenzani, "Common Architectures and Devices for Current Source Inverter in Motor-Drive Applications: A Comprehensive Review," *Energies*, vol. 16, no. 15, 2023. [Online]. Available: https://www.mdpi.com/1996-1073/16/15/5645

[28] B. H. Zacher, A. Bauer, K. Franck, and C. Schumann, "48 V Current Source Inverter with Bidirectional GaN eHEMT Switches for Low Inductance Machine Drives," in *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe)*, 2023, pp. 1–9.

[29] Nexperia, "Bi-directional GaN FETs," 2024. [Online]. Available: https://www.nexperia.com/products/gan-fets/bi-directional-gan-fets

[30] Y. Zhang, "Investigation of Approaches for Improving the Performance and Fault Tolerance of Permanent Magnet Synchronous Machine Drives Using Current-Source Inverters," PhD Thesis, University of Wisconsin-Madison, 2016.

[31] X. Yang, Z. Zhao, C. Wang, J. Xu, K. Liu, and J. Qiu, "Analysis and Parameter Design of SiC-Based Current Source Inverter (CSI)," *World Electric Vehicle Journal*, vol. 13, no. 10, 2022.

[32] B. Riegler and A. Muetze, "Passive Component Optimization for Current-Source-Inverters," *IEEE Transactions on Industry Applications*, vol. 59, no. 5, pp. 6113–6124, 2023.

[33] P. Li, J. Zhang, J. Wang, and X. Cai, "A new design method for the dc inductance in current source converters," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, 2016, pp. 3160–3165.

[34] P. Song, Y. Liu, and C. Liu, "Research on parameter design and control method for current source inverter–fed im drive systems," *Machines*, vol. 10, no. 10, 2022. [Online]. Available: https://www.mdpi.com/2075-1702/10/10/922

[35] X. Li, Y. Sun, L. Jiang, S. Xie, Y. Liu, and M. Su, "A Modulation Scheme to Reduce Leakage Current of Split-Capacitor Four-Wire Current Source Inverter," *IEEE Transactions on Power Electronics*, vol. 38, no. 10, pp. 13 156–13 165, 2023.

[36] X. Guo, Y. Yang, and X. Wang, "Optimal Space Vector Modulation of Current-Source Converter for DC-Link Current Ripple Reduction," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 1671–1680, 2019.

[37] Q. Lei and F. Z. Peng, "Space Vector Pulsewidth Amplitude Modulation for a Buck–Boost Voltage/Current Source Inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 266–274, 2014.

[38] Z. Bai, Z. Zhang, and Y. Zhang, "A Generalized Three-Phase Multilevel Current Source Inverter with Carrier Phase-Shifted SPWM," in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 2055–2060.

[39] Taufik, Y. Tam, and M. Anwari, "Comparative study of sinusoidal pulse width and hysteresis modulations in current source inverter," in *2007 International Conference on Intelligent and Advanced Systems*, 2007, pp. 906–911.

[40] M. Baumann, T. Nussbaumer, and J. Kolar, "Comparative evaluation of modulation methods of a three-phase buck+boost pwm rectifier. part i: Theoretical analysis," *IET Power Electronics*, vol. 1, pp. 255–267, 2008. [Online]. Available: https://digital-library.theiet.org/doi/abs/10.1049/iet-pel%3A20070123

[41] T. Nussbaumer, M. Baumann, and J. Kolar, "Comparative evaluation of modulation methods of a three-phase buck+boost pwm rectifier. part ii: Experimental verification," *IET Power Electronics*, vol. 1, pp. 268–274, 2008. [Online]. Available: https://digital-library.theiet.org/doi/abs/10.1049/iet-pel%3A20070124

[42] Plexim, "Current Source Inverter," May 2023. [Online]. Available: https://www.plexim.com/sites/default/files/demo_models_categorized/tic2000/current_source_inverter.pdf

[43] X. Tan, J. Dai, and B. Wu, "A novel converter configuration for wind applications using PWM CSI with diode rectifier and buck converter," in *2011 IEEE*

International Electric Machines & Drives Conference (IEMDC), 2011, pp. 359–364.

[44] H. A. Moghaddam and A. Ramezankhani, "Comparative Performance Analysis of Constant and Variable DC Bus Current CSI-Fed PMSM Drive in a Wide Range of Speed and Torque," in *2023 3rd International Conference on Electrical Machines and Drives (ICEMD)*, 2023, pp. 1–8.

[45] Y. Lee and A. Castellazzi, "Implementation options of a fully SiC Buck-CSI for advanced motor drive application," in *2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe)*, 2022, pp. P.1–P.11.

[46] H.-C. Chen and H.-H. Huang, "Design of buck-type current source inverter fed brushless DC motor drive and its application to position sensorless control with square-wave current," *IET Electric Power Applications*, vol. 7, no. 5, 2013.

[47] E. Gurpinar, F. Iannuzzo, Y. Yang, A. Castellazzi, and F. Blaabjerg, "Design of Low-Inductance Switching Power Cell for GaN HEMT Based Inverter," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1592–1601, 2018.

[48] M. Ul Hassan, Y. Wu, A. Imran Emon, Z. Yuan, and F. Luo, "Design Considerations and Their Optimization for a Two-Level GaN-Based Current Source Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 3, pp. 3173–3187, 2024.

[49] E. Sayed, M. Abdalmagid, G. Pietrini, N.-M. Sa'adeh, A. D. Callegaro, C. Goldstein, and A. Emadi, "Review of Electric Machines in More-/Hybrid-/Turbo-Electric Aircraft," *IEEE Transactions on Transportation Electrification*, vol. 7, no. 4, pp. 2976–3005, 2021.

[50] C. Liu, K. T. Chau, C. H. T. Lee, and Z. Song, "A Critical Review of Advanced Electric Machines and Control Strategies for Electric Vehicles," *Proceedings of the IEEE*, vol. 109, no. 6, pp. 1004–1028, 2021.

[51] C. Gerada, M. Galea, and A. Kladas, "Electrical machines for aerospace applications," in *2015 IEEE Workshop on Electrical Machines Design, Control and Diagnosis (WEMDCD)*, 2015, pp. 79–84.

[52] S. Sakunthala, R. Kiranmayi, and P. N. Mandadi, "A study on industrial motor drives: Comparison and applications of PMSM and BLDC motor drives," in

2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS), 2017, pp. 537–540.

[53] F. Kelch, Y. Yang, B. Bilgin, and A. Emadi, "Investigation and design of an axial flux permanent magnet machine for a commercial midsize aircraft electric taxiing system," *IET Electrical Systems in Transportation*, vol. 8, no. 1, pp. 52–60, 2018. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-est.2017.0039

[54] T. Marcel and D. S. Ioan, "Design of an Electronic Direct Drive Automotive Differential using Axial Flux PSMS with Sensorless Direct Torque and Flux Control," in *2022 International Conference and Exposition on Electrical And Power Engineering (EPE)*, 2022, pp. 078–083.

[55] M. Polat, A. Yildiz, and R. Akinci, "Performance Analysis and Reduction of Torque Ripple of Axial Flux Permanent Magnet Synchronous Motor Manufactured for Electric Vehicles," *IEEE Transactions on Magnetics*, vol. 57, no. 7, pp. 1–9, 2021.

[56] W. Zhao, T. A. Lipo, and B.-I. Kwon, "Comparative Study on Novel Dual Stator Radial Flux and Axial Flux Permanent Magnet Motors With Ferrite Magnets for Traction Application," *IEEE Transactions on Magnetics*, vol. 50, no. 11, pp. 1–4, 2014.

[57] B. Zhang, T. Epskamp, M. Doppelbauer, and M. Gregor, "A comparison of the transverse, axial and radial flux PM synchronous motors for electric vehicle," in *2014 IEEE International Electric Vehicle Conference (IEVC)*, 2014, pp. 1–6.

[58] M. Aydin and M. Gulec, "A New Coreless Axial Flux Interior Permanent Magnet Synchronous Motor With Sinusoidal Rotor Segments," *IEEE Transactions on Magnetics*, vol. 52, no. 7, pp. 1–4, 2016.

[59] B. Anvari, P. Guedes-Pinto, and R. Lee, "Dual Rotor Axial Flux Permanent Magnet Motor using PCB Stator," in *2021 IEEE International Electric Machines & Drives Conference (IEMDC)*, 2021, pp. 1–7.

[60] F. Tokgoz, Gülsuna, F. Karakaya, G. Cakal, and O. Keysan, "Mechanical and Thermal Design of an Optimized PCB Motor for an Integrated Motor Drive System With GaNFETs," *IEEE Transactions on Energy Conversion*, vol. 38, no. 1, pp. 653–661, 2023.

[61] N. S., S. P. Nikam, S. Singh, S. Pal, A. K. Wankhede, and B. G. Fernandes, "High-Speed Coreless Axial-Flux Permanent-Magnet Motor With Printed Circuit Board Winding," *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 1954–1962, 2019.

[62] J. Zhao, Y. Wang, T. Ma, X. Liu, and J. Li, "Losses and Thermal Analysis of an Integrated PCB Coreless Axial Flux PMSM with the Drive System," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 11, pp. 11 022–11 032, 2023.

[63] X. Wang, C. Hu, M. Zhao, L. Wu, and S. Zhou, "Design of multi-layer PCB coreless axial permanent magnet synchronous motor," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, 2019, pp. 1–4.

[64] D.-W. Nam, M.-K. Hong, N.-R. Jo, D.-H. Jung, and W.-H. Kim, "Design of Coil Patterns for an Axial Flux Permanent Magnet Synchronous Motor with PCB Stator," *IEEE Access*, pp. 1–1, 2025.

[65] X. Wang, C. Li, and F. Lou, "Geometry Optimize of Printed Circuit Board Stator Winding in Coreless Axial Field Permanent Magnet Motor," in *2016 IEEE Vehicle Power and Propulsion Conference (VPPC)*, 2016, pp. 1–6.

[66] ECM PCB Stator Tech, "PCB Stator Technology," 2025. [Online]. Available: https://pcbstator.com/pcb-stator-technology/

[67] Celestica, "Celestica Partners with ECM to Bring their Patented Technology Solutions to the Aerospace and Defense Market," October 2021. [Online]. Available: https://corporate.celestica.com/news-releases/news-release-details/celestica-partners-ecm-bring-their-patented-technology-solutions

[68] East West, "ECM and East West Partner on PCB Stator Electric Motor Production," June 2024. [Online]. Available: https://www.ewmfg.com/about/news/east-west-and-ecm-announce-strategic-partnership/

[69] E. Gilmore, "Infinitum Secures $185 Million Series E Funding Led by Just Climate to Catalyze Industrial Decarbonization with High-Efficiency, Sustainable Motors," 2023. [Online]. Available: https://www.businesswire.com/news/home/20231101739350/en

[70] X. Wang, T. Li, P. Gao, and X. Zhao, "Design and Loss Analysis of Axial Flux Permanent Magnet Synchronous Motor with PCB Distributed Winding,"

in *2021 24th International Conference on Electrical Machines and Systems (ICEMS)*, 2021, pp. 1112–1117.

[71] S. Asgari, N. Saed, and A. Muetze, "Enhancing PCB Motor Performance through Phase Resistance Reduction in Slotted PCB Motors with Ferrite Core," in *2023 26th International Conference on Electrical Machines and Systems (ICEMS)*, 2023, pp. 3780–3784.

[72] ——, "Low-Cost Axial Flux PCB Motor with Ferrite Core and Ferrite Magnet Topology for Fan Applications," in *2023 IEEE International Electric Machines & Drives Conference (IEMDC)*, 2023, pp. 1–5.

[73] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 2nd ed. John Wiley & Sons, Inc., 1995.

[74] U. Waleed, M. Waseem, H. Shaukat, A. Ijaz, A. Almalaq, and M. A. Mohamed, "An Efficient FPGA Based Scalar V/f Control Mechanism of Three Phase Induction Motor for Electric Vehicles," in *2021 31st Australasian Universities Power Engineering Conference (AUPEC)*, 2021, pp. 1–6.

[75] E. Rajlaxmi, S. Behera, and S. K. Panda, "Comparison of Inverter Control by SPWM and SVPWM Method in Standalone PV System," in *2020 IEEE International Symposium on Sustainable Energy, Signal Processing and Cyber Security (iSSSC)*, 2020, pp. 1–6.

[76] K. B. Tawfiq, P. Sergeant, and A. S. Mansour, "Comparative Analysis of Space Vector Pulse-Width Modulation Techniques of Three-Phase Inverter to Minimize Common Mode Voltage and/or Switching Losses," *Mathematics*, vol. 12, no. 18, 2024. [Online]. Available: https://www.mdpi.com/2227-7390/12/18/2832

[77] A. Yang, M. Lin, L. Jia, and K. Lin, "A Modified Rotor Flux Observer Based Sensorless Method for Dual Three-Phase PMSM," in *2023 IEEE International Conference on Applied Superconductivity and Electromagnetic Devices (ASEMD)*, 2023, pp. 1–2.

[78] G. Wang, M. Valla, and J. Solsona, "Position Sensorless Permanent Magnet Synchronous Machine Drives—A Review," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 7, pp. 5830–5842, 2020.

[79] Z. Wang, K. Yu, Y. Li, and M. Gu, "Position Sensorless Control of Dual Three-Phase IPMSM Drives With High-Frequency Square-Wave Voltage Injection," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 10, pp. 9925–9934, 2023.

[80] Y. Wu, R. McMahon, Y. Zhan, and A. Knight, "Impact of PWM Schemes on Induction Motor Losses," in *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, vol. 2, 2006, pp. 813–818.

[81] A. Boglietti, P. Ferraris, M. Lazzari, and M. Pastorelli, "Influence of the inverter characteristics on the iron losses in PWM inverter-fed induction motors," *IEEE Transactions on Industry Applications*, vol. 32, no. 5, pp. 1190–1194, 1996.

[82] J.-J. Lee, Y.-K. Kim, H. Nam, K.-H. Ha, J.-P. Hong, and D.-H. Hwang, "Loss distribution of three-phase induction motor fed by pulsewidth-modulated inverter," *IEEE Transactions on Magnetics*, vol. 40, no. 2, pp. 762–765, 2004.

[83] X. Fan, W. Li, and Q. Ke, "Hysteresis-Based Mechanism Analysis of Iron Loss Increment Caused by PWM Harmonics in Permanent Magnet Synchronous Motor," in *2024 IEEE 7th International Electrical and Energy Conference (CIEEC)*, 2024, pp. 3785–3790.

[84] C. Simao, N. Sadowski, N. Batistela, and J. Bastos, "Analysis of Magnetic Hysteresis Loops under Sinusoidal and PWM Voltage Waveforms," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 1555–1559.

[85] J. Ma, H. Liu, H. Ma, and Z. Bai, "A novel hysteresis loss calculation method of filter inductor in PWM inverters," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, 2013, pp. 287–292.

[86] X. Gao, N. Duan, W. Xu, S. Huang, and S. Wang, "Hysteresis Modeling and Measurement of Oriented Silicon Steel Under PWM Excitation," in *2022 IEEE 20th Biennial Conference on Electromagnetic Field Computation (CEFC)*, 2022, pp. 1–2.

[87] J. Espinoza and G. Joos, "A current-source-inverter-fed induction motor drive system with reduced losses," *IEEE Transactions on Industry Applications*, vol. 34, no. 4, pp. 796–805, 1998.

[88] H.-C. Chen and H.-H. Huang, "Design of buck-type current source inverter fed brushless dc motor drive and its application to position sensorless control with square-wave current," *IET Electric Power Applications*, vol. 7, no. 5, pp. 416–426, 2013. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-epa.2013.0002

[89] D. Benatti, G. Migliazza, E. Carfagna, F. Immovilli, and E. Lorenzani, "Novel Single-Stage Current Source Inverter: Extension to Low-Speed Region in Motor Drive Applications," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 9, pp. 10 335–10 345, 2024.

[90] M. J. Mauger, P. Kandula, and D. Divan, "Soft-Switching Current Source Inverter for Next-Generation Electric Vehicle Drivetrains," in *2020 IEEE Transportation Electrification Conference & Expo (ITEC)*, 2020, pp. 651–658.

[91] W. Taha and M. Narimani, "A Modified Current Source Inverter Fed Drive for Electric Vehicle Applications," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 822–828.

[92] J. Styles, "Common misconceptions about the body diode," *Design World: Power & Energy Efficiency Handbook*, pp. 12–14, October 2019.

[93] GaN Systems Inc., "GN012 Application Note: Gate Driver Circuit Design with GaN E-HEMTs," March 2022. [Online]. Available: https://gansystems.com/wp-content/uploads/2022/03/GN012_Gate-Driver-Design-with-GaN-E-HEMTs_220308.pdf

[94] F. Y. Fu, "GaN Power HEMT Tutorial: GaN Driving," October 2019. [Online]. Available: https://iganpower.com/wp-content/uploads/2019/10/GaN-Power-Device-Tutorial-Part2-GaN-Driving.pdf

[95] Nexperia, "Gate drive circuit design for Nexperia 650 V Enhancementmode (e-mode) GaN FETs," May 2023. [Online]. Available: https://assets.nexperia.com/documents/application-note/AN90041.pdf

[96] YESvGaN, "YESvGaN," 2025. [Online]. Available: https://www.yesvgan.eu/en

[97] W. J. Zhang, Y. Leng, J. Yu, X. Jiang, C. Cheng, and W. T. Ng, "Gate driver IC for enhancement mode GaN power transistors with senseFET reverse conduction detection circuit," *IET Power Electronics*,

vol. 12, no. 15, pp. 3928–3935, 2019. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-pel.2018.6381

[98] T. Morita, M. Yanagihara, H. Ishida, M. Hikita, K. Kaibara, H. Matsuo, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "650 V 3.1 mcm2 GaN-based monolithic bidirectional switch using normally-off gate injection transistor," in *2007 IEEE International Electron Devices Meeting*, 2007, pp. 865–868.

[99] H. Umeda, Y. Yamada, K. Asanuma, F. Kusama, Y. Kinoshita, H. Ueno, H. Ishida, T. Hatsuda, and T. Ueda, "High power 3-phase to 3-phase matrix converter using dual-gate GaN bidirectional switches," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 894–897.

[100] S. Musumeci, M. Panizza, F. Stella, and F. Perraud, "Monolithic Bidirectional Switch Based on GaN Gate Injection Transistors," in *2020 IEEE 29th International Symposium on Industrial Electronics (ISIE)*, 2020, pp. 1045–1050.

[101] R. A. Torres, H. Dai, W. Lee, T. M. Jahns, and B. Sarlioglu, "Development of Current-Source-Inverter-based Integrated Motor Drives using Wide-Bandgap Power Switches," in *2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)*, 2019, pp. 1–6.

[102] R. Amorim Torres, H. Dai, W. Lee, B. Sarlioglu, and T. Jahns, "Current-Source Inverter Integrated Motor Drives Using Dual-Gate Four-Quadrant Wide-Bandgap Power Switches," *IEEE Transactions on Industry Applications*, vol. 57, no. 5, pp. 5183–5198, 2021.

[103] H. Dai, R. A. Torres, W. Lee, T. M. Jahns, and B. Sarlioglu, "Integrated Motor Drive using Soft-Switching Current-Source Inverters with SiC- and GaN-based Bidirectional Switches," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 2372–2378.

[104] H. Dai, T. M. Jahns, R. A. Torres, M. Liu, B. Sarlioglu, and S. Chang, "Development of High-Frequency WBG Power Modules with Reverse-Voltage-Blocking Capability for an Integrated Motor Drive using a Current-Source Inverter," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1808–1815.

[105] M. ul Hassan, A. I. Emon, Z. Yuan, H. Peng, and F. Luo, "Performance Comparison and Modelling of Instantaneous Current Sharing Amongst GaN HEMT Switch Configurations for Current Source Inverters," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 2014–2020.

[106] Mustafeez-Ul-Hassan, Y. Wu, Y. Li, A. Muneeb, and F. Luo, "Reverse Voltage Blocking Switches Using Paralleled GaN Devices for Current Source Inverter Applications," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 6510–6515.

[107] R. A. Torres, H. Dai, T. M. Jahns, and B. Sarlioglu, "Operation and Analysis of Current-Source Inverters using Dual-Gate Four-Quadrant Wide-Bandgap Power Switches," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2353–2360.

[108] Texas Instruments, "LAUNCHXL-F28379D," March 2022. [Online]. Available: https://www.ti.com/tool/LAUNCHXL-F28379D

[109] Infineon Technologies, "GS-065-030-6-LR 700 V E-mode GaN transistor Datasheet," 2024. [Online]. Available: https://www.mouser.ca/datasheet/2/196/Infineon_GS_065_030_6_LR_TR_DataSheet_v01_00_EN-3440058.pdf

[110] J. Chen, Q. Luo, Y. Wei, X. Zhang, and X. Du, "The Sustained Oscillation Modeling and Its Quantitative Suppression Methodology for GaN Devices," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7927–7941, 2021.

[111] Skyworks, "Si827x Data Sheet," July 2022. [Online]. Available: https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/data-sheets/Si827x.pdf

[112] Diodes Incorporated, "Bootstrap Capacitor Considerations," January 2016. [Online]. Available: https://www.diodes.com/assets/App-Note-Files/DN1153_Bootstrap_Capacitor_Considerations.pdf

[113] Skyworks, "AN486: High-Side Bootstrap Design Using ISODrivers in Power Delivery Systems," October 2021. [Online]. Available: https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/application-notes/AN486.pdf

[114] GaN Systems Inc., "GN010 Application Note EZDrive® Power Stage Solution for GaN Systems' GaN Transistor," July 2022.

[Online]. Available: https://gansystems.com/wp-content/uploads/2022/07/GN010-ENG-EZDrive-Solution-for-GaN-Systems-GaN-Transistors-Rev.220720.pdf

[115] Texas Instruments, "TMCS1123 Precision 250kHz Hall-Effect Current Sensor With Reinforced Isolation Working Voltage, Overcurrent Detection and Ambient Field Rejection," January 2025. [Online]. Available: https://www.ti.com/lit/ds/symlink/tmcs1123.pdf?ts=1720724795965

[116] F. Chen, S. Lee, T. M. Jahns, and B. Sarlioglu, "Comprehensive Comparative Analysis: VSI-based vs. CSI-based Motor Drive Systems with Sinusoidal Output Voltage," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 1021–1027.

[117] National Instruments, "Protecting NI Switch Modules When Switching Inductive Loads," July 2018. [Online]. Available: https://knowledge.ni.com/KnowledgeArticleDetails?id=kA00Z000000kKOZSA2

[118] PCBWay, "PCBWay Custom Design Rules," May 2024. [Online]. Available: https://www.pcbway.com/helpcenter/design_instruction/PCBWay_Custom_Design_Rules.html

[119] Bittele Electronics Inc., "PCB Trace Width Calculator," 2025. [Online]. Available: https://www.7pcb.com/trace-width-calculator

[120] L. Rozenblat, "Calculating Spacing Between PCB Traces for Various Voltage Levels," 2014. [Online]. Available: https://www.smps.us/pcbtracespacing.html

[121] Gan Systems Inc., "GN002 Application Note: Thermal Design for GaNPX® Packaged Devices," July 2021. [Online]. Available: https://gansystems.com/wp-content/uploads/2021/10/GN002_Thermal-Design-Guide-for-Top-Side-Cooled-GaNpx-T-Devices_Rev-210720.pdf

[122] ——, "PCB Thermal Design Guide for GaN Enhancement Mode Power Transistors," 2016. [Online]. Available: https://gansystems.com/wp-content/uploads/2018/01/GN005_PCB-Thermal-Design-Guide-Enhancement-Mode-031815.pdf

[123] Mia, "PCBWay Upgrades PCB Material to ShengYi Material," May 2024. [Online]. Available: https://www.pcbway.com/blog/3/PCBWay_Upgrades_Multi_Layers_PCB_Material_to_ShengYi_Material_d4ba6d1c.html

[124] Infineon Technologies, "EiceDRIVER™ 1EDBx275F," November 2021. [Online]. Available: https://www.infineon.com/dgdl/Infineon-1EDB8275F-DataSheet-v02_02-EN.pdf?fileId=8ac78c8c7d0d8da4017d2c9fc1dd6c0b

[125] Gan Systems Inc., "GN003 Application Note: Measurement Techniques for High-Speed GaN E-HEMTs," March 2022. [Online]. Available: https://gansystems.com/wp-content/uploads/2022/03/GN003-Measurement-Techniques-for-High-Speed-GaN-E-HEMTs_220308.pdf

[126] O. Trescases, G. Wei, A. Prodic, and W. T. Ng, "Predictive Efficiency Optimization for DC–DC Converters With Highly Dynamic Digital Loads," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1859–1869, 2008.

[127] S. J. Chapman, *Electric Machinery Fundamentals*, 5th ed. New York: McGraw-Hill, 2012.

[128] A. Allca-Pekarovic, P. J. Kollmeyer, J. Reimers, P. Mahvelatishamsabadi, T. Mirfakhrai, P. Naghshtabrizi, and A. Emadi, "Loss Modeling and Testing of 800-V DC Bus IGBT and SiC Traction Inverter Modules," *IEEE Transactions on Transportation Electrification*, vol. 10, no. 2, pp. 2923–2935, 2024.